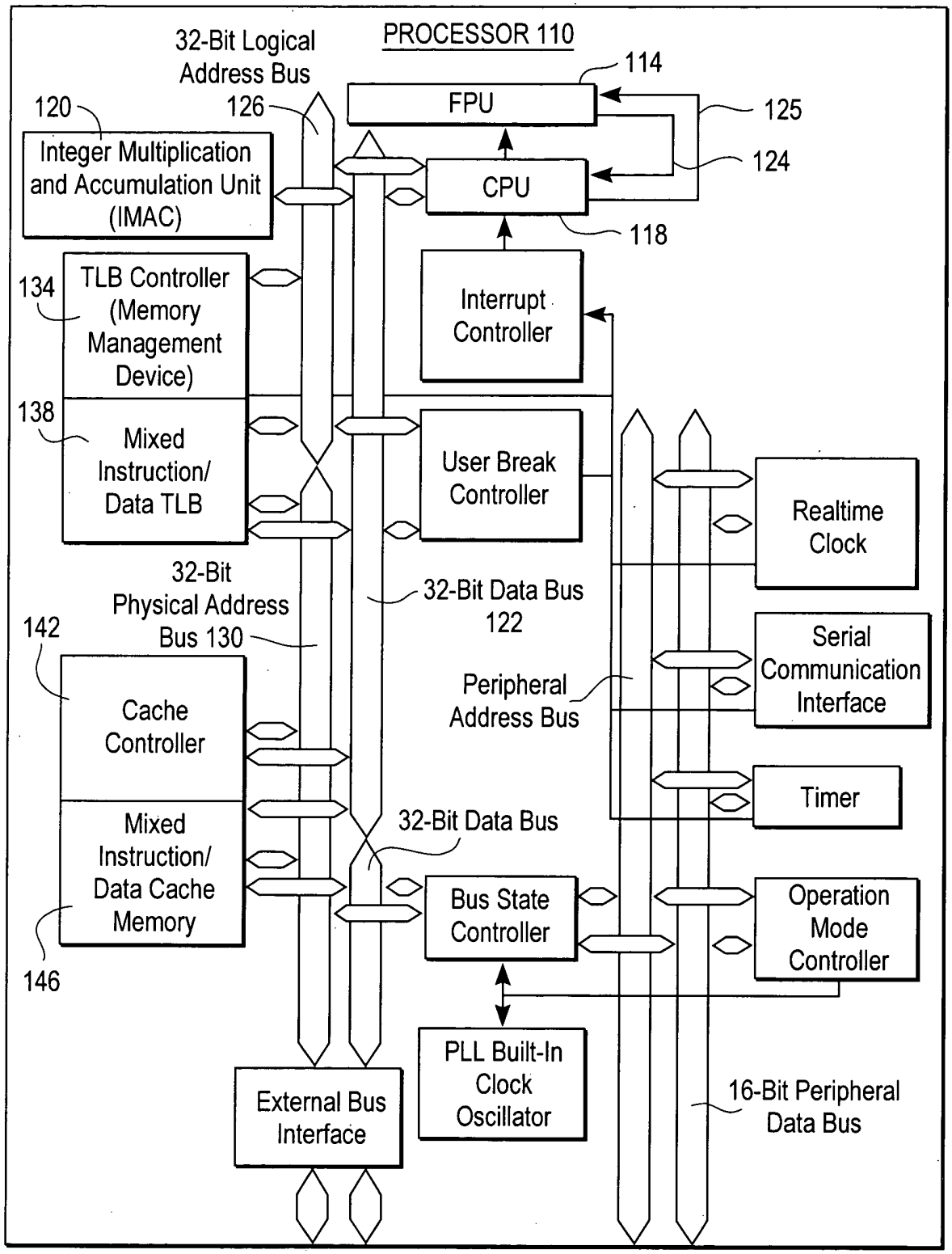

PROCESSOR 110
32-Bit Logical Address Bus
126
120
Integer Multiplication and Accumulation Unit (IMAC)
114
FPU
125
124
CPU
118
Interrupt Controller
134
TLB Controller (Memory Management Device)
138
Mixed Instruction/ Data TLB
User Break Controller
Realtime Clock
32-Bit Physical Address Bus 130
32-Bit Data Bus 122
142
Cache Controller
Peripheral Address Bus
Serial Communication Interface
Timer
Mixed Instruction/ Data Cache Memory
146
32-Bit Data Bus
Bus State Controller
Operation Mode Controller
PLL Built-In Clock Oscillator
External Bus Interface
16-Bit Peripheral Data Bus

FIG. 1

FPU AND CPU PIPELINES USED TO EXECUTE INSTRUCTIONS

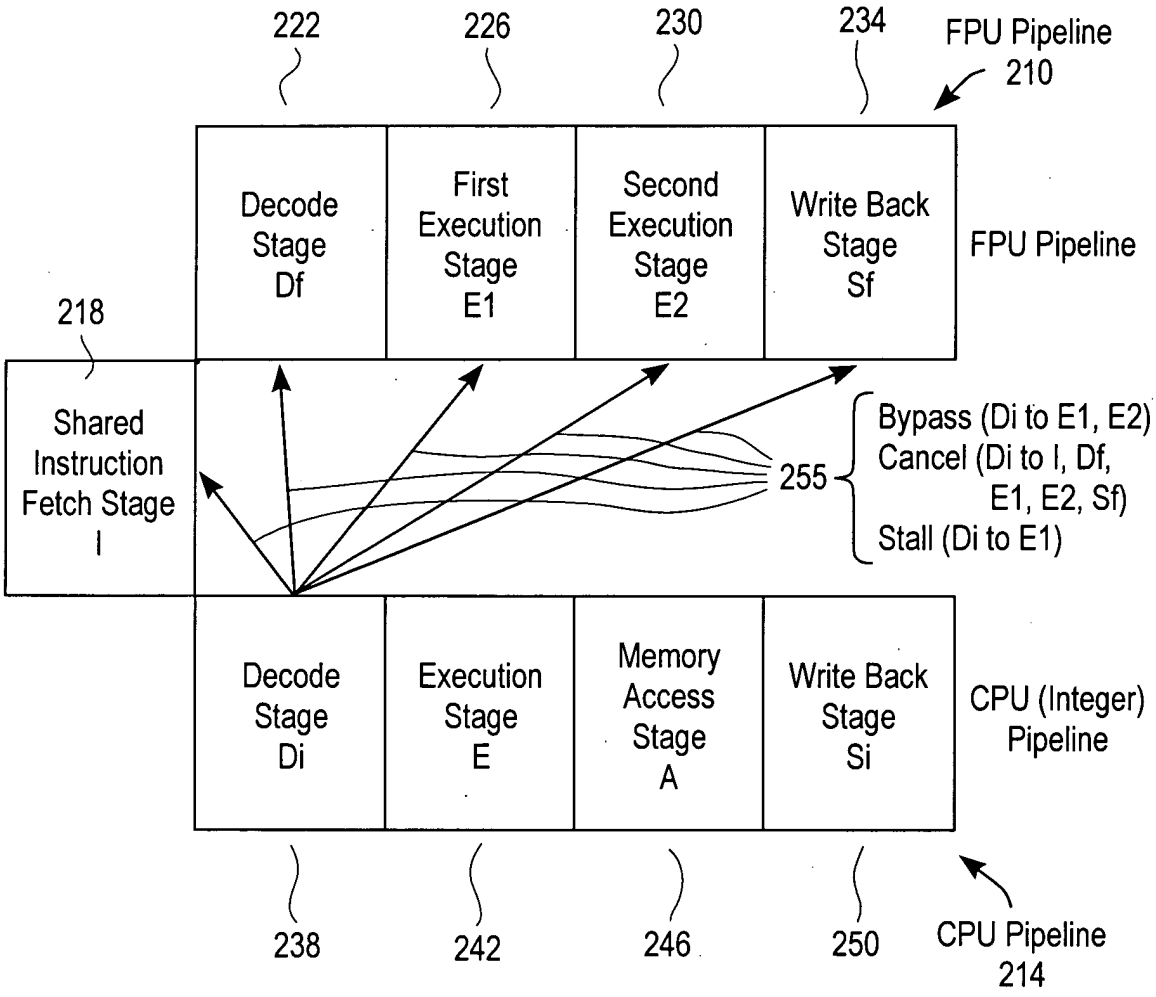


FIG. 2

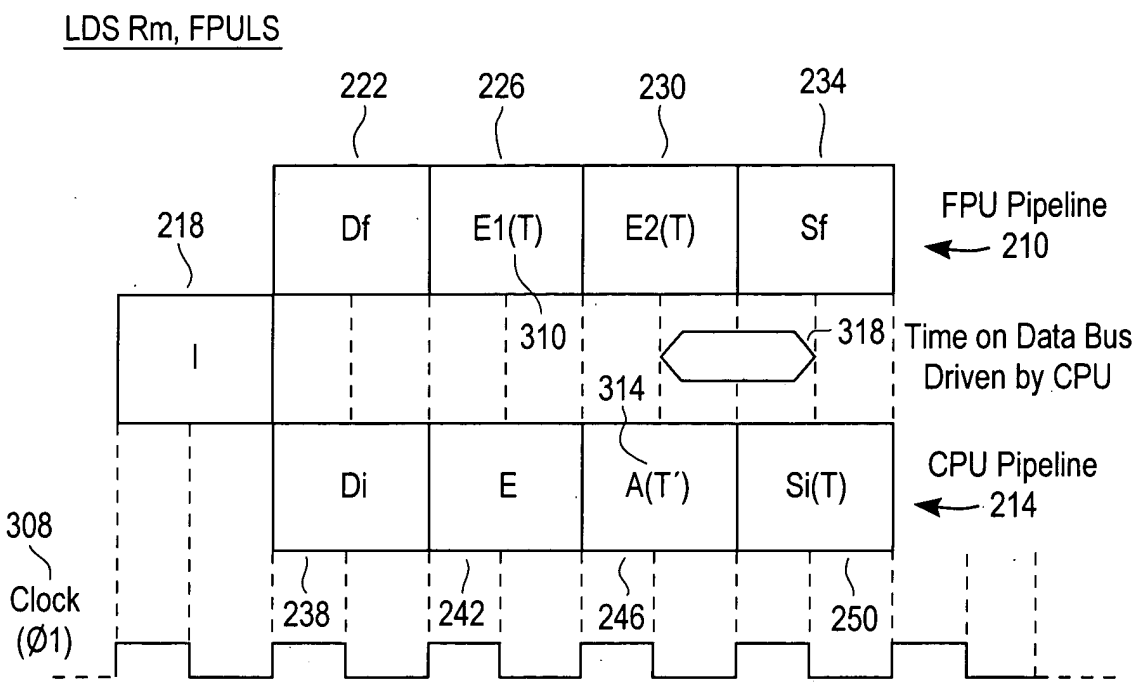

LDS Rm, FPULS
222
226
230
234
218
Df
E1(T)
E2(T)
Sf
FPU Pipeline
210
I
310
318
Time on Data Bus
Driven by CPU
314
Di
E
A(T')
Si(T)
CPU Pipeline
214
308
Clock
(Ø1)
238
242
246
250

FIG. 3(a)

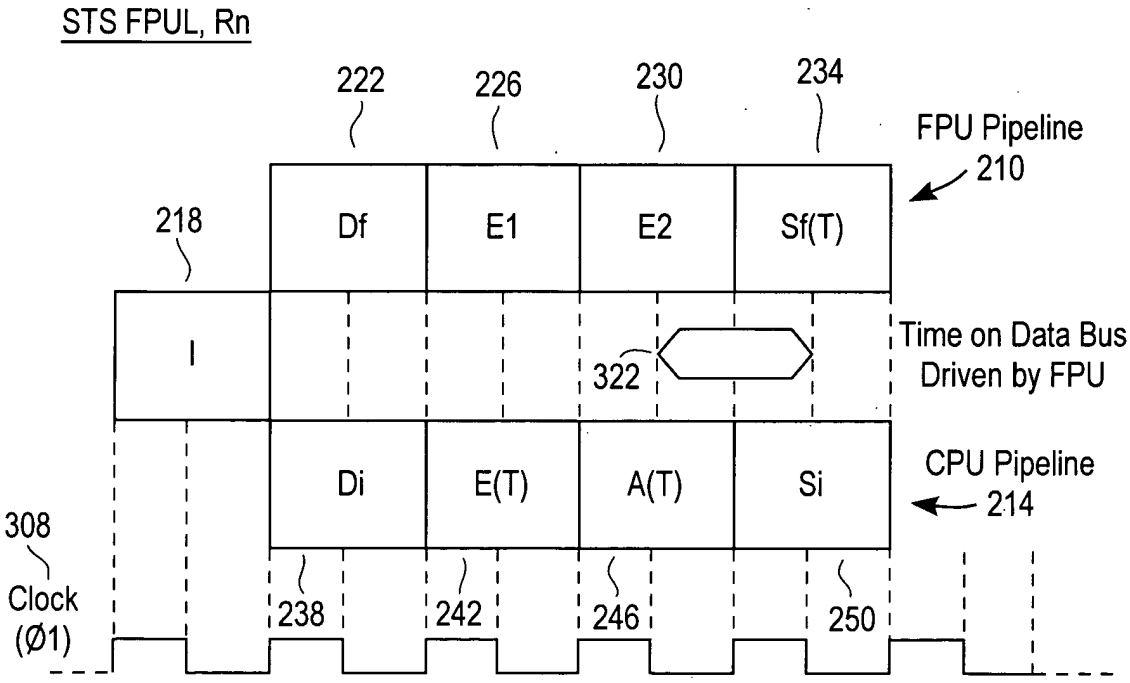

STS FPUL, Rn
222
226
230
234
FPU Pipeline
210
218
Df
E1
E2
Sf(T)
I
322
Time on Data Bus
Driven by FPU
Di
E(T)
A(T)
Si
CPU Pipeline
214
308
Clock
(Ø1)
238
242
246
250

FIG. 3(b)

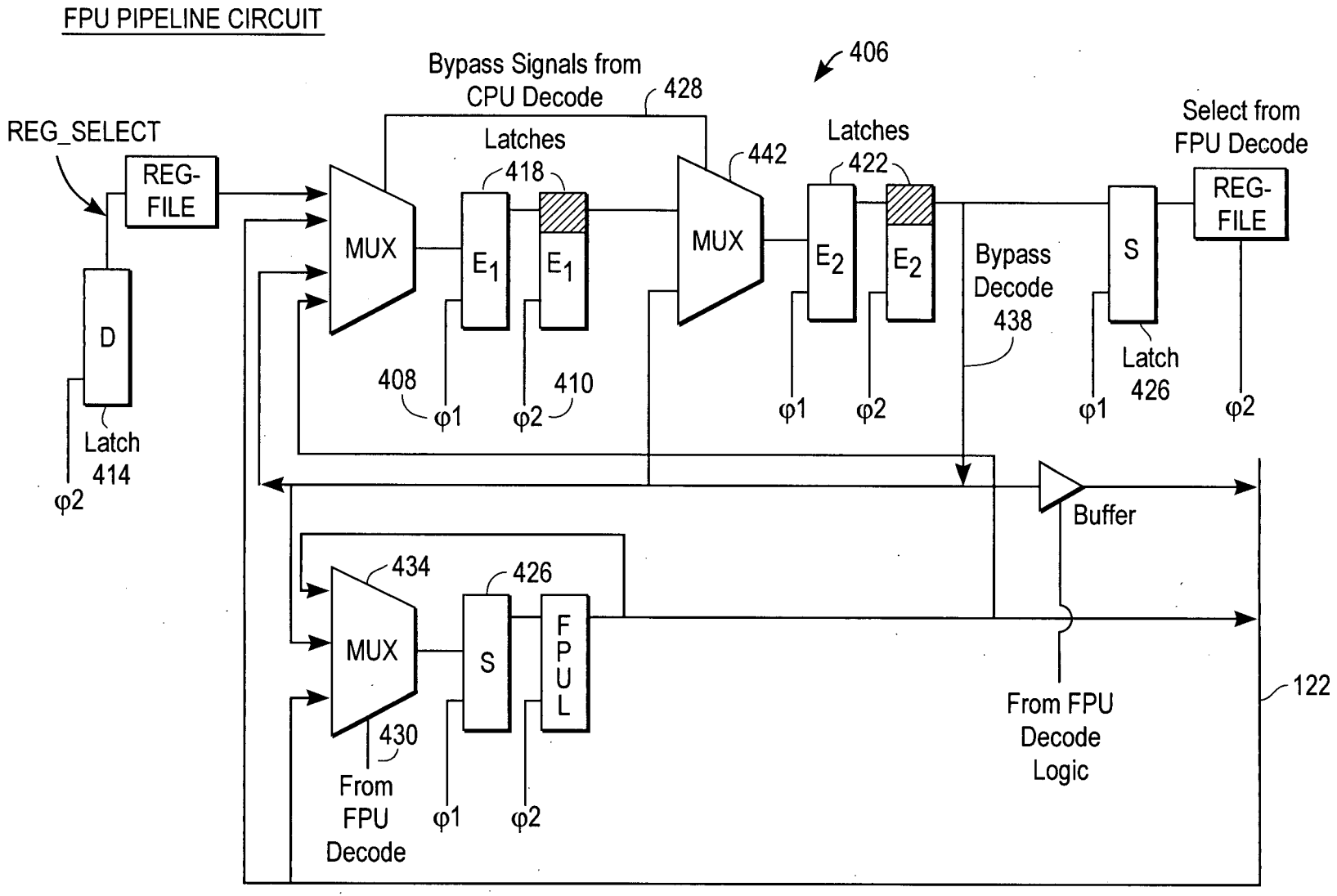

FPU PIPELINE CIRCUIT
406
Bypass Signals from CPU Decode
428
REG_SELECT
REG-FILE
Latches
418
442
Latches
422
Select from FPU Decode
REG-FILE
MUX
E1
E1
MUX
E2
E2
Bypass Decode
438
S
D
Latch 414
φ2
408
φ1
φ2
410
φ1
φ2
φ1
Latch 426
φ2
Buffer
434
426
MUX
S
FPUL
430
From FPU Decode
φ1
φ2
From FPU Decode Logic
122

FIG. 4

SYNCHRONIZATION OF PIPELINE RESOURCE SHARING

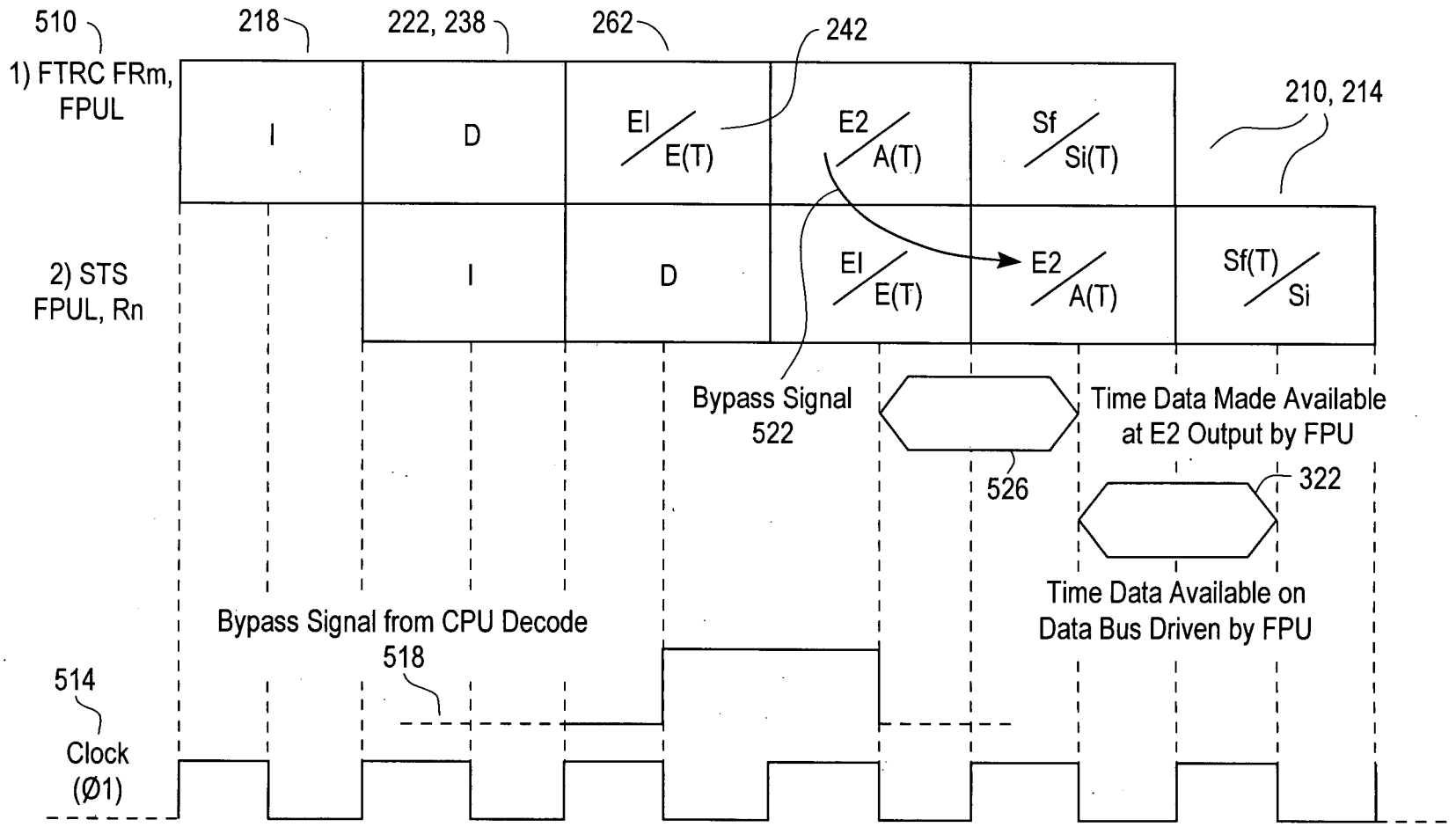


FIG. 5

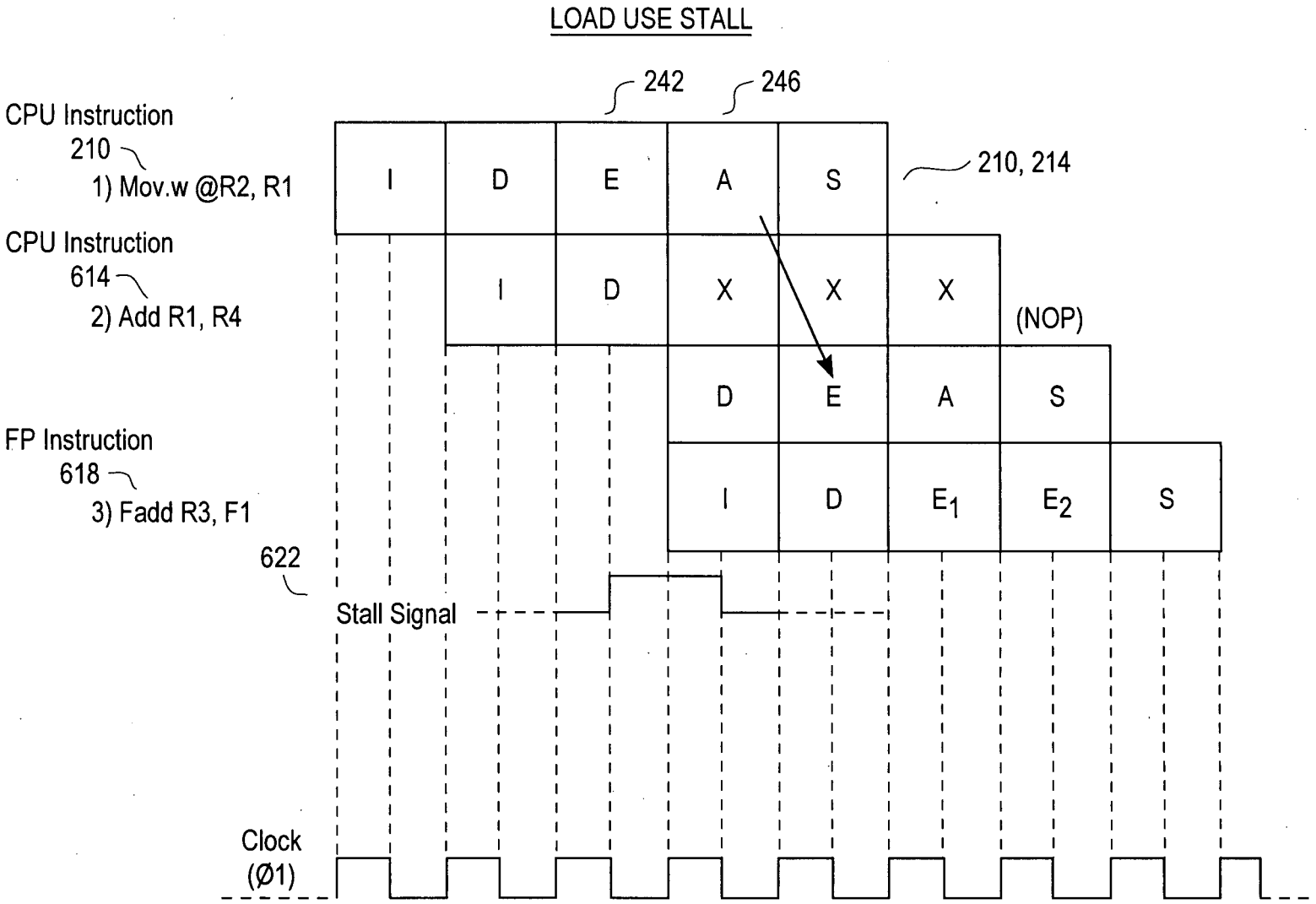

LOAD USE STALL
242
246
CPU Instruction
210
1) Mov.w @R2, R1
I
D
E
A
S
210, 214
CPU Instruction
614
2) Add R1, R4
I
D
X
X
X
(NOP)
D
E
A
S
FP Instruction
618
3) Fadd R3, F1
I
D
E1
E2
S
622
Stall Signal
Clock
(Ø1)

FIG. 6

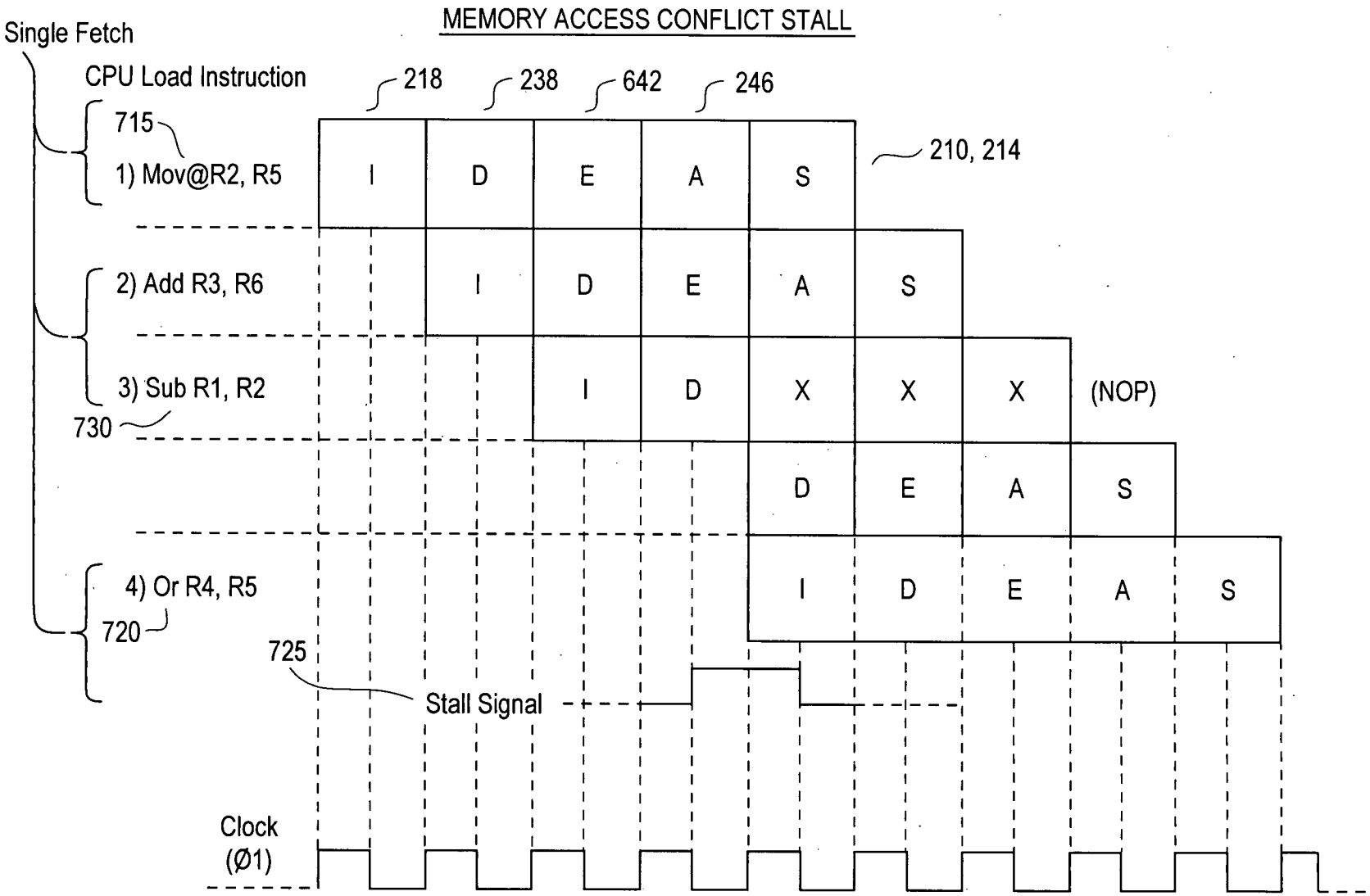

MEMORY ACCESS CONFLICT STALL
Single Fetch
CPU Load Instruction
715
1) Mov@R2, R5
2) Add R3, R6
3) Sub R1, R2
730
4) Or R4, R5
720
218
238
642
246
210, 214
I D E A S
I D E A S
I D X X X (NOP)
D E A S
I D E A S
725
Stall Signal
Clock
(Ø1)

FIG. 7

STALL SIGNAL GENERATION CIRCUIT

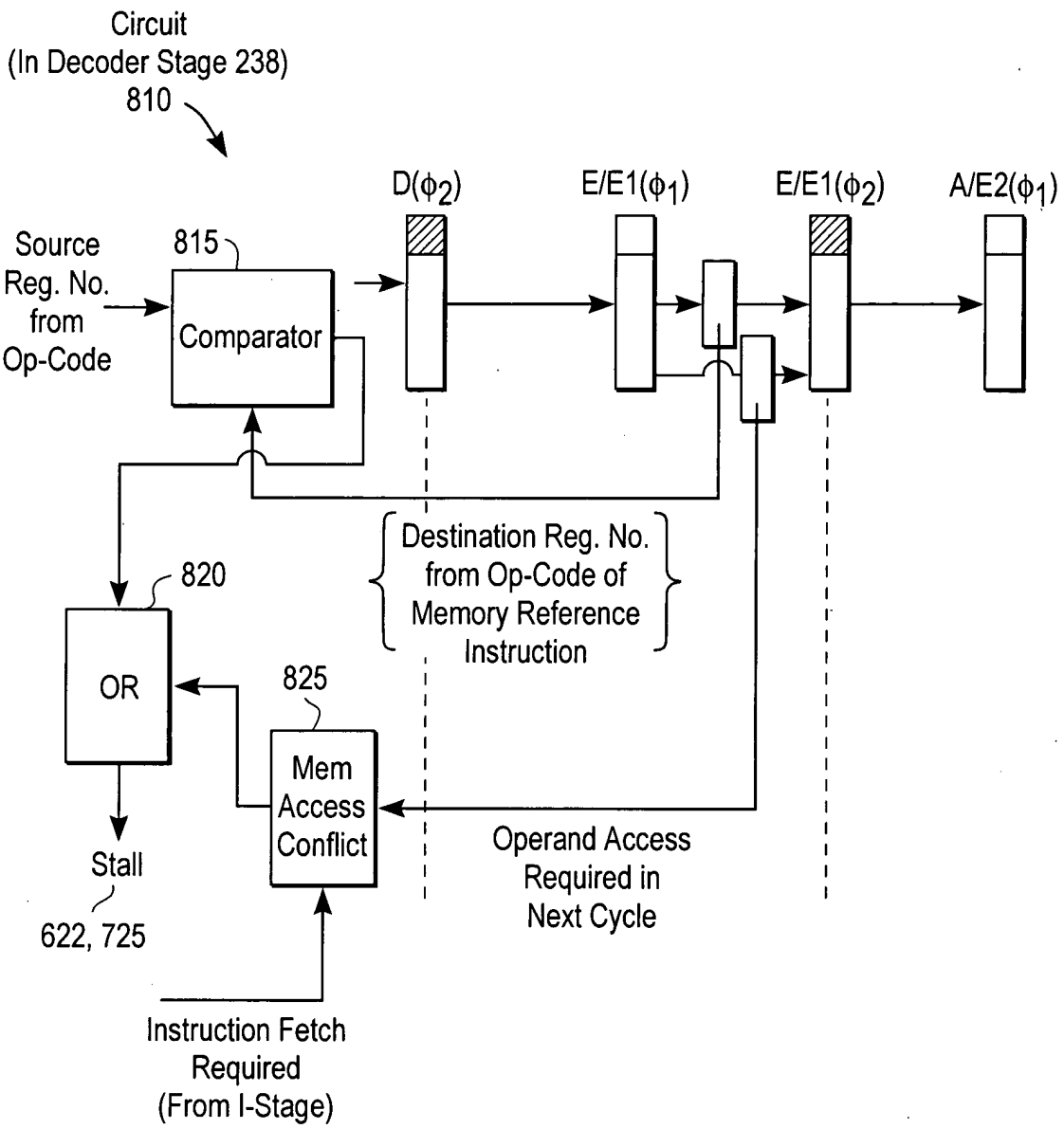


FIG. 8

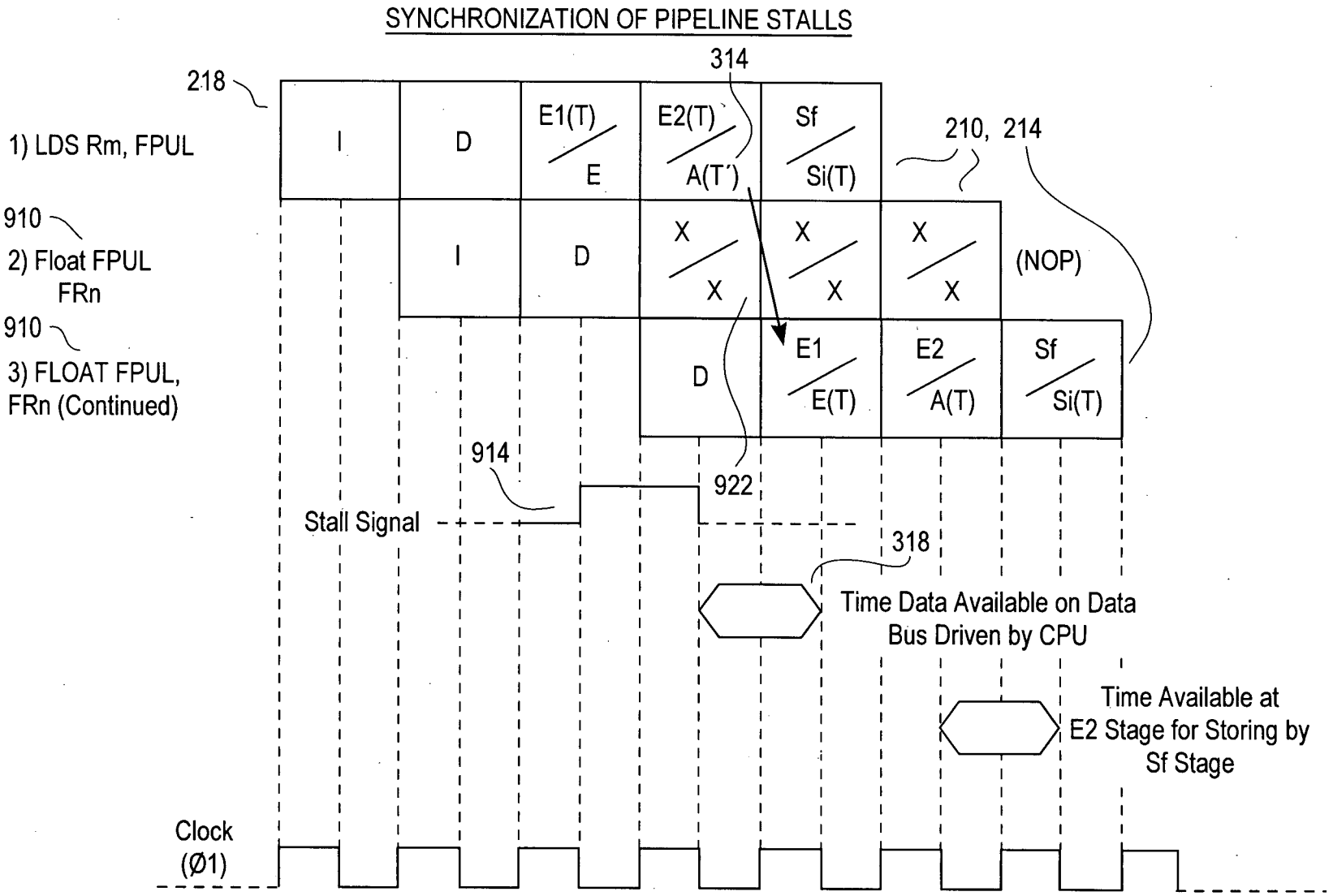

SYNCHRONIZATION OF PIPELINE STALLS
218
314
1) LDS Rm, FPUL
I
D
E1(T) / E
E2(T) / A(T')
Sf / Si(T)
210, 214
910
2) Float FPUL FRn
I
D
X / X
X / X
X / X
(NOP)
910
3) FLOAT FPUL, FRn (Continued)
D
E1 / E(T)
E2 / A(T)
Sf / Si(T)
914
922
Stall Signal
318
Time Data Available on Data Bus Driven by CPU
Time Available at E2 Stage for Storing by Sf Stage
Clock (Ø1)

FIG. 9

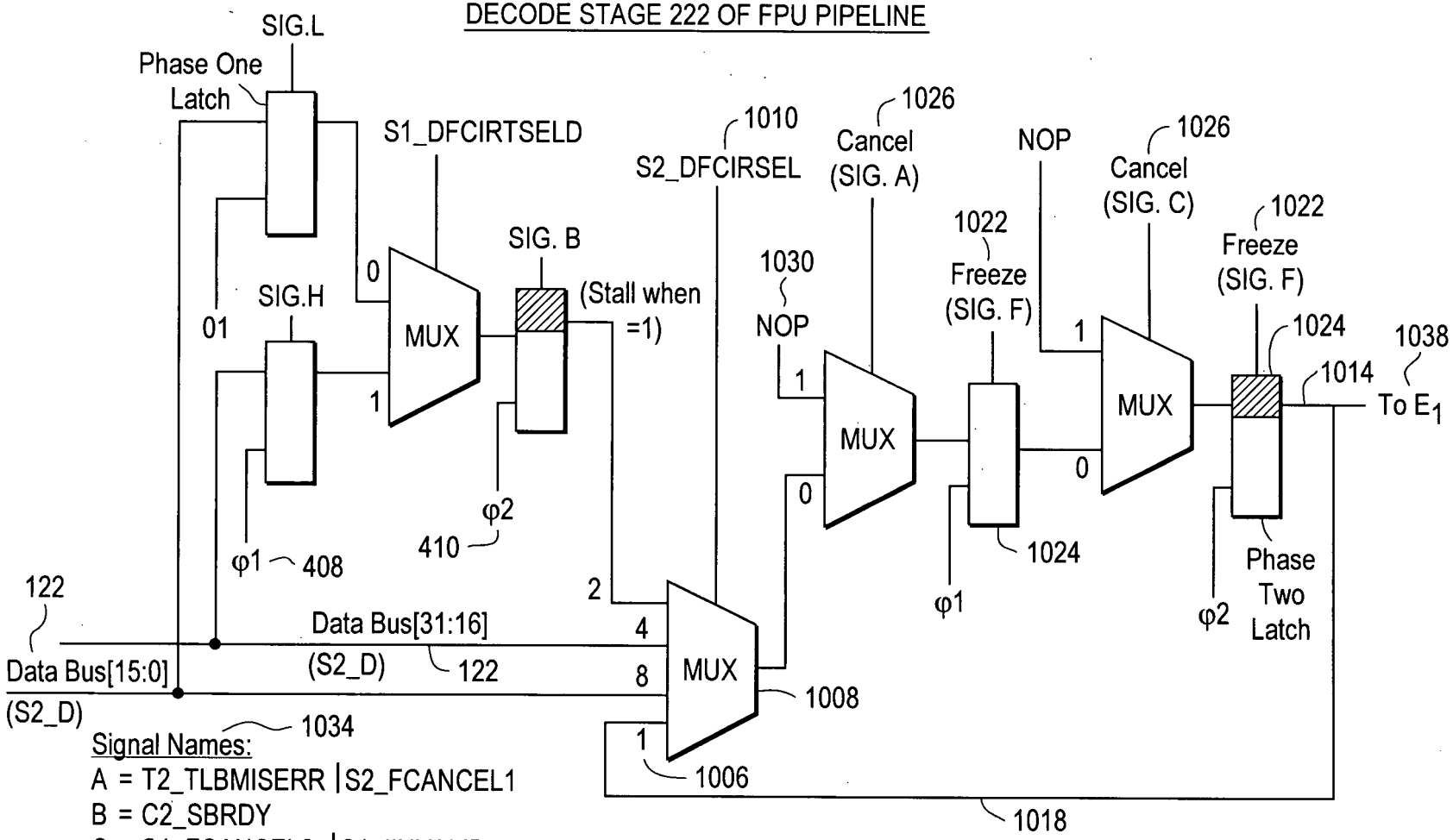
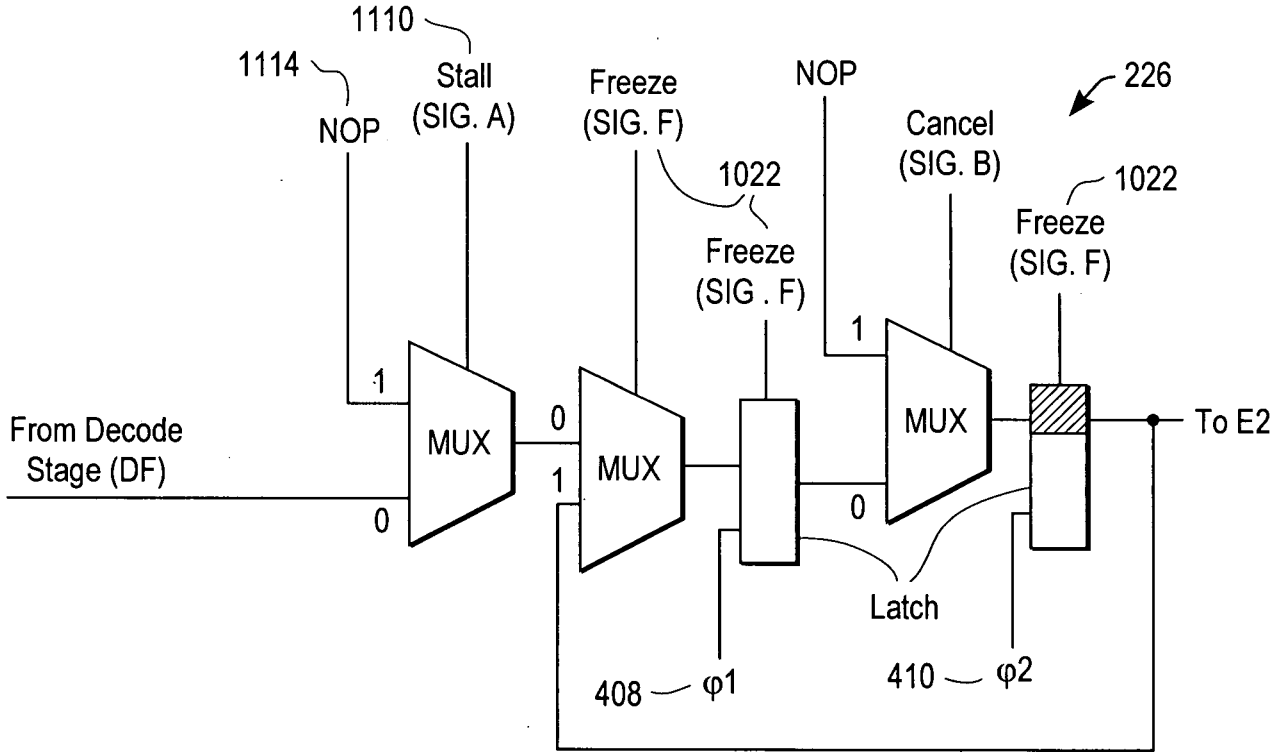

DECODE STAGE 222 OF FPU PIPELINE
SIG.L
Phase One Latch
S1_DFCIRTSELD
1010
S2_DFCIRSEL
1026
Cancel (SIG. A)
NOP
1026
Cancel (SIG. C)
1022
Freeze (SIG. F)
1022
Freeze (SIG. F)
SIG. B
(Stall when =1)
1030
NOP
SIG.H
01
MUX
0
1
MUX
MUX
MUX
MUX
1024
1014
1038
To E1
φ2
410
φ1
408
φ1
φ2
1024
Phase Two Latch
122
Data Bus[31:16]
(S2_D)
122
Data Bus[15:0]
(S2_D)
2
4
8
1008
1
1006
1018
1034
Signal Names:
A = T2_TLBMISERR |S2_FCANCEL1
B = C2_SBRDY
C = S1_FCANCEL2 |S1_IINVALID
F = (C2_SBRDY & L2_LRDY)
L = S2_IRTHILL & C2_SBRDY & L2_LRDY
H = S2_IRTHIHL & C2_SBRDY & L2_LRDY

FIG. 10

FIRST EXECUTIONS STAGE (E1) OF FPU PIPELINE



1114

Signal Names:

A = (T2_TLBMISERR & ~ FPU_IFETCH) |S2_FSTALL |~FDIV_STEP |(C2_SBRDY & L2_LRDY)

B = S1_FCANCEL2

F = (C2_SBRDY & L2_LRDY)

FIG. 11

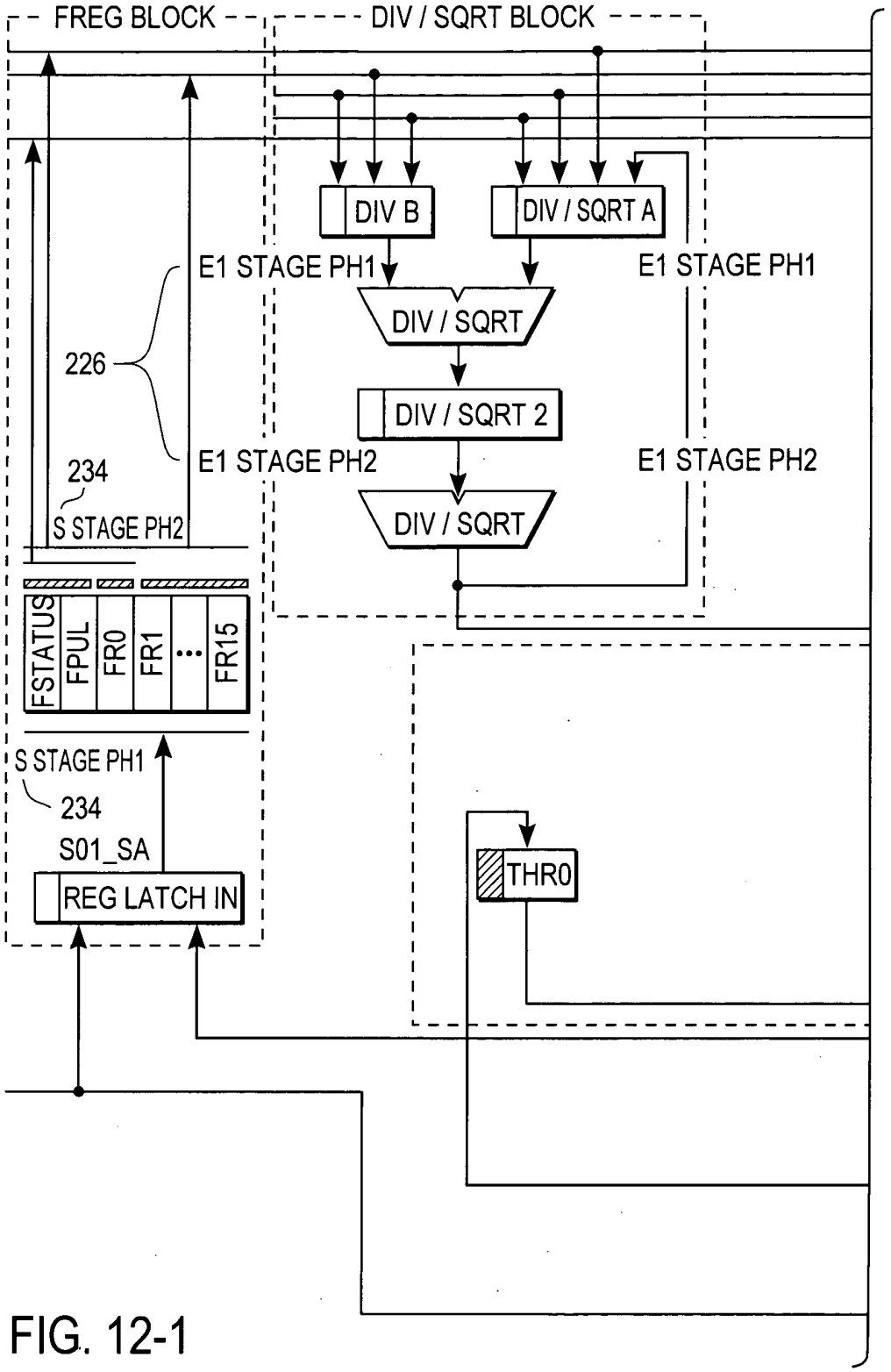
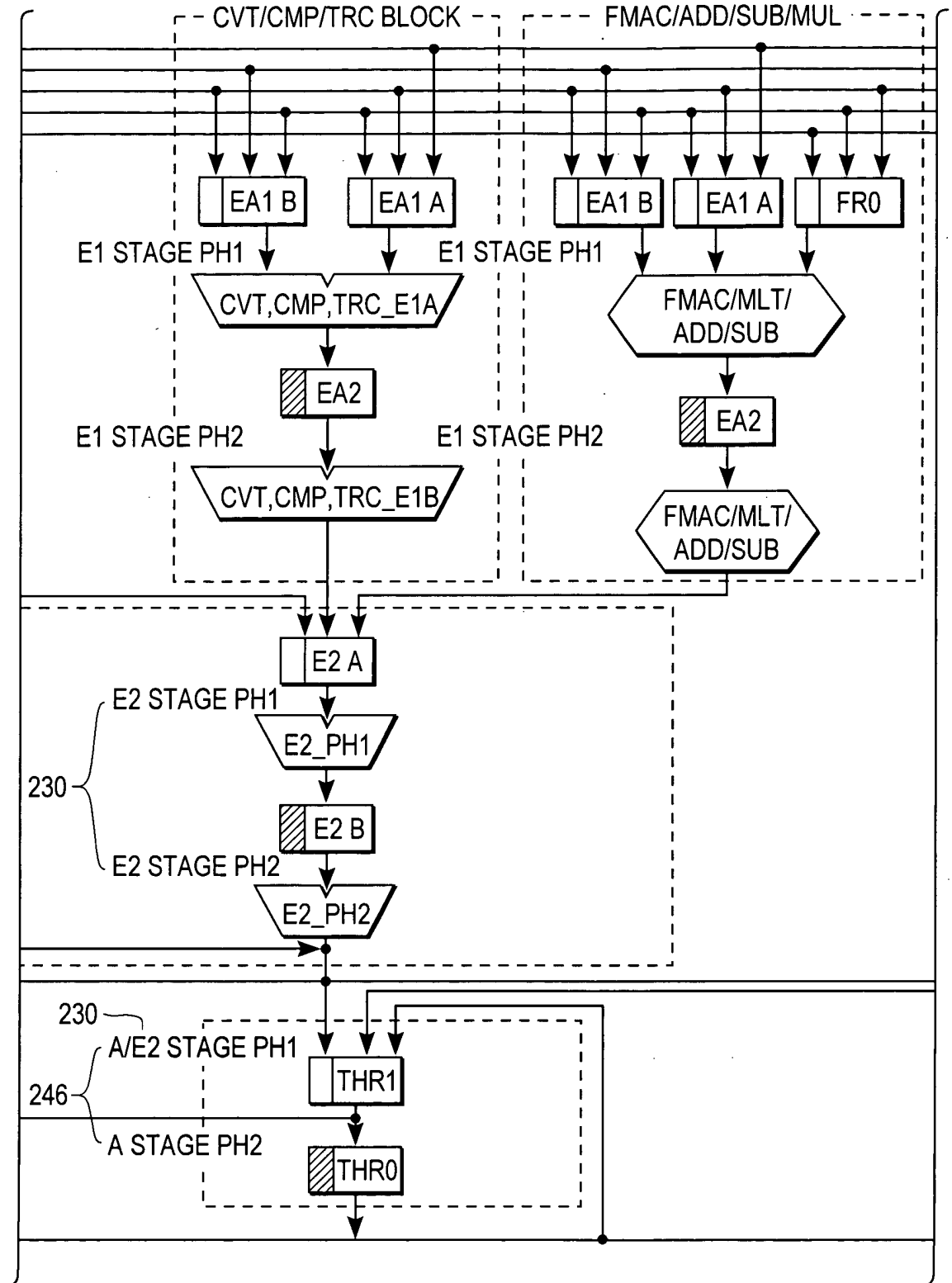


FIG. 12-1

FIG. 12-2 →



← FIG. 12-1

FIG. 12-2

FIG. 12-3 →

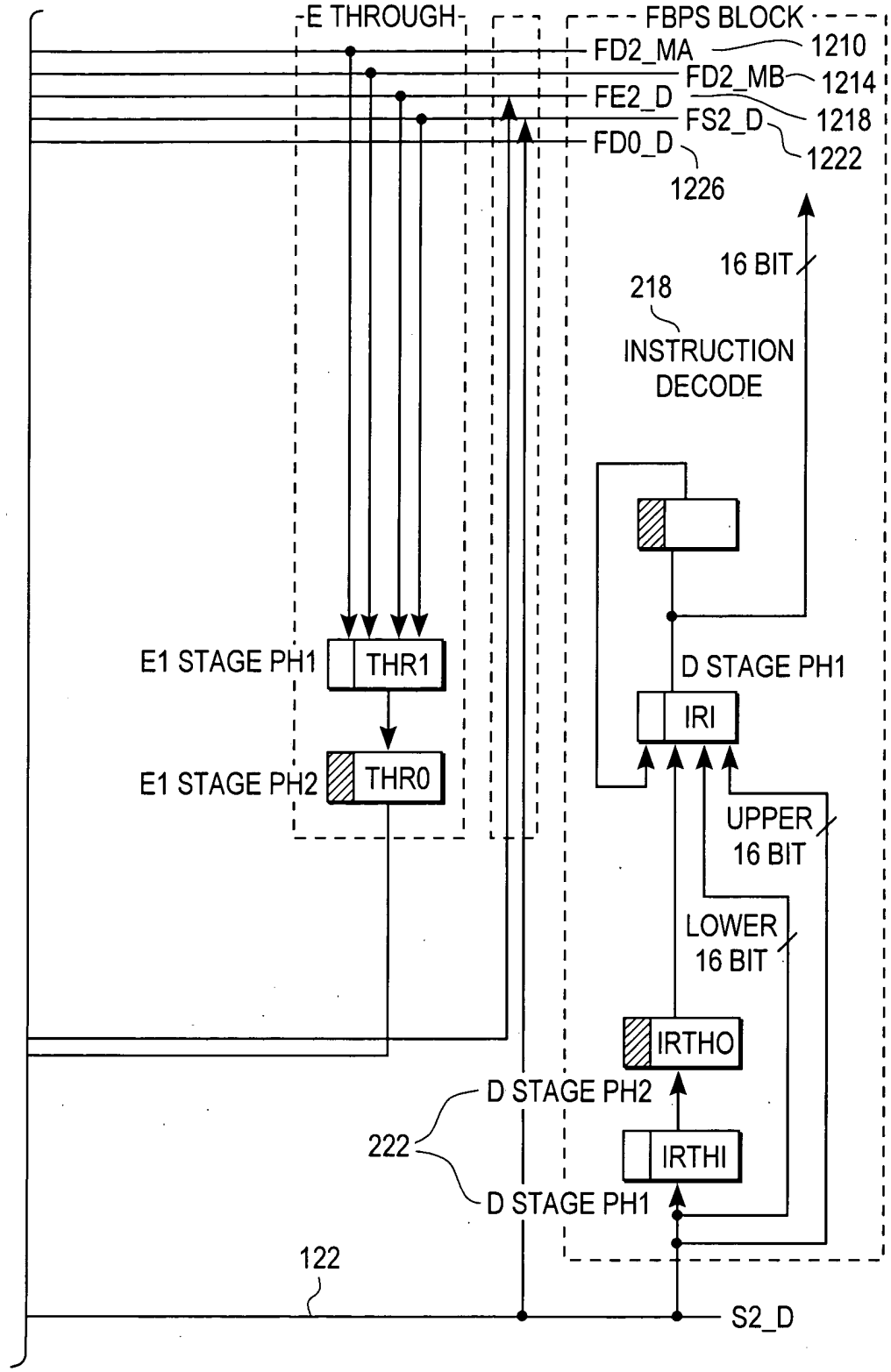


FIG. 12-2

FIG. 12-3

T-BIT BYPASSING

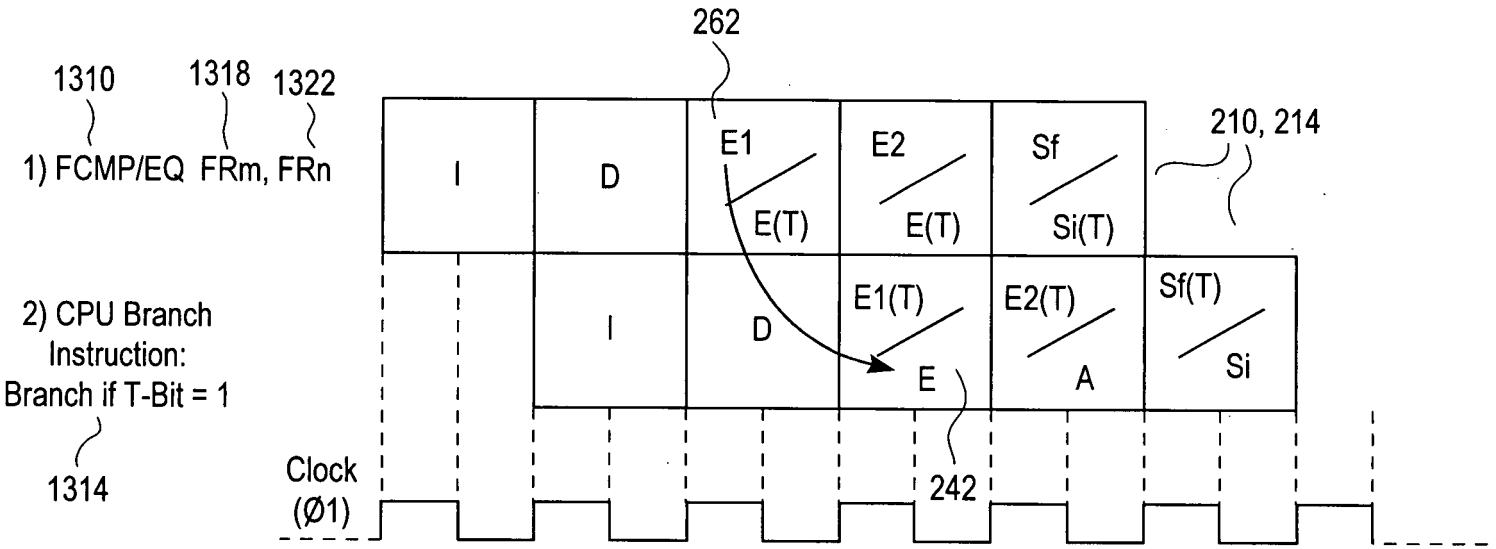


FIG. 13

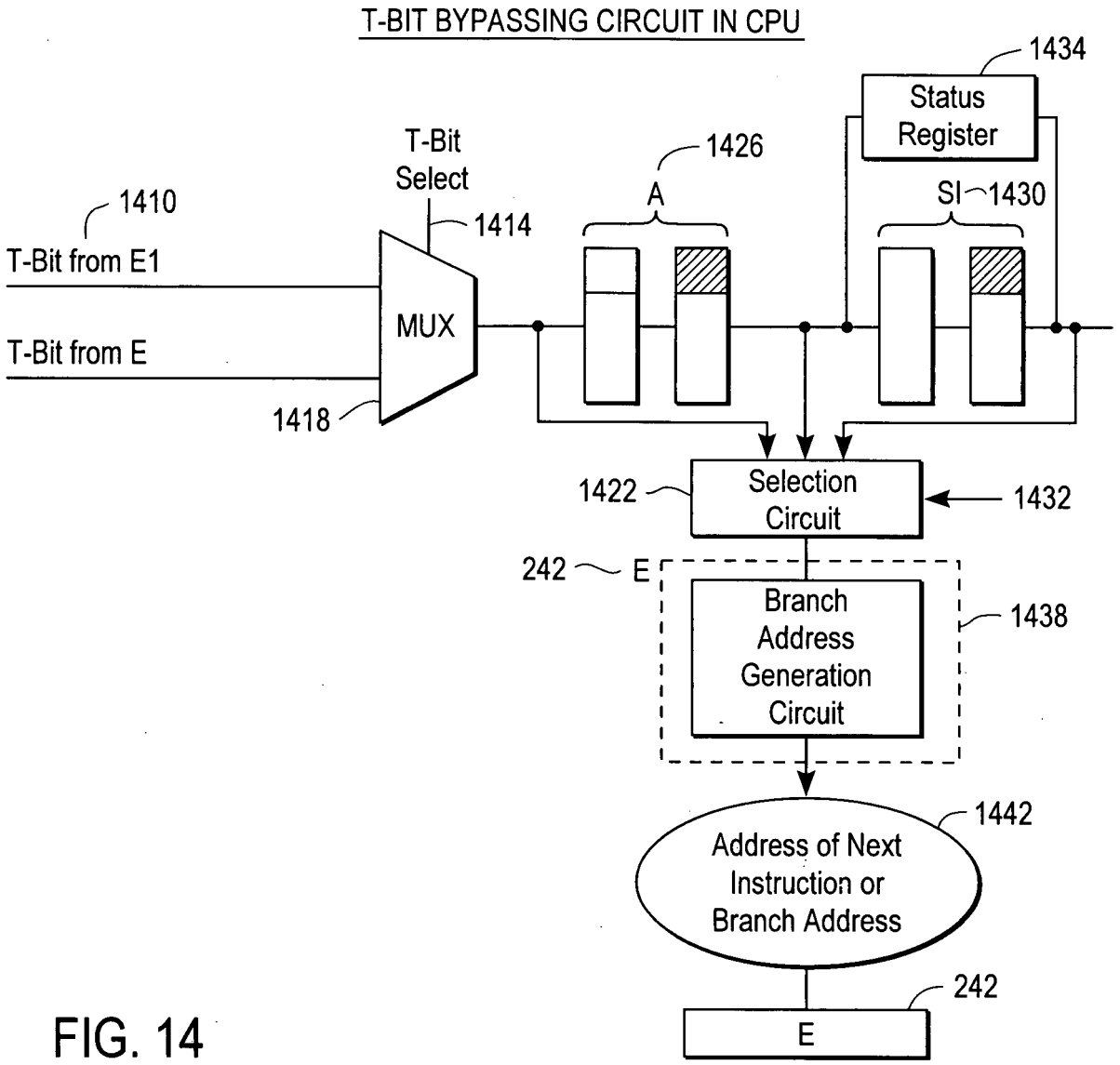

T-BIT BYPASSING CIRCUIT IN CPU
1434
Status Register
T-Bit Select
1426
A
SI
1430
1410
1414
T-Bit from E1
T-Bit from E
MUX
1418
1422
Selection Circuit
1432
242
E
Branch Address Generation Circuit
1438
1442
Address of Next Instruction or Branch Address
242
E

FIG. 14

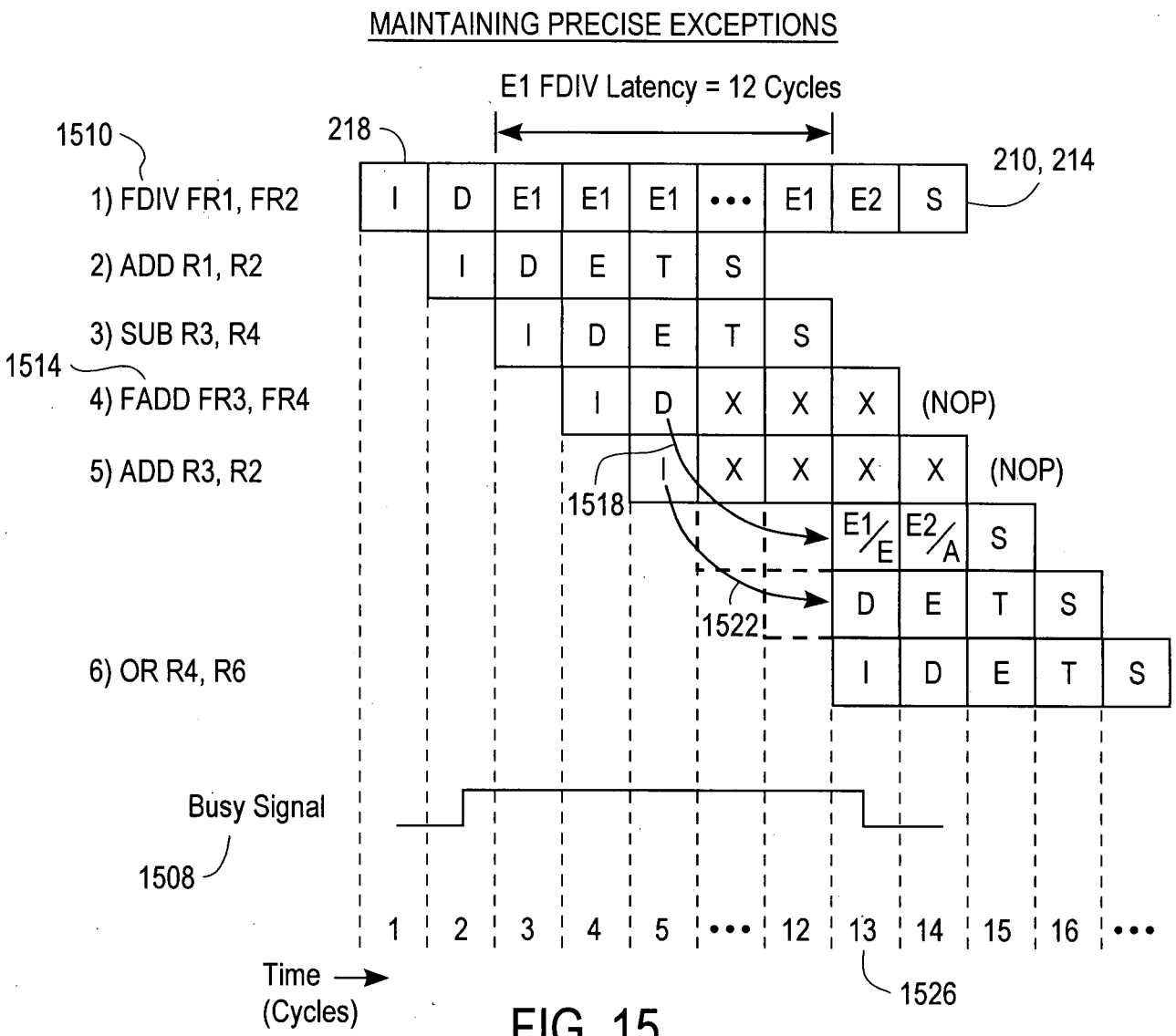

MAINTAINING PRECISE EXCEPTIONS
E1 FDIV Latency = 12 Cycles
1510
218
210, 214
1) FDIV FR1, FR2
I D E1 E1 E1 ••• E1 E2 S
2) ADD R1, R2
I D E T S
3) SUB R3, R4
I D E T S
1514
4) FADD FR3, FR4
I D X X X (NOP)
5) ADD R3, R2
I X X X X (NOP)
1518
E1/E E2/A S
D E T S
1522
6) OR R4, R6
I D E T S
Busy Signal
1508
1 2 3 4 5 ••• 12 13 14 15 16 •••
Time (Cycles)
1526

FIG. 15

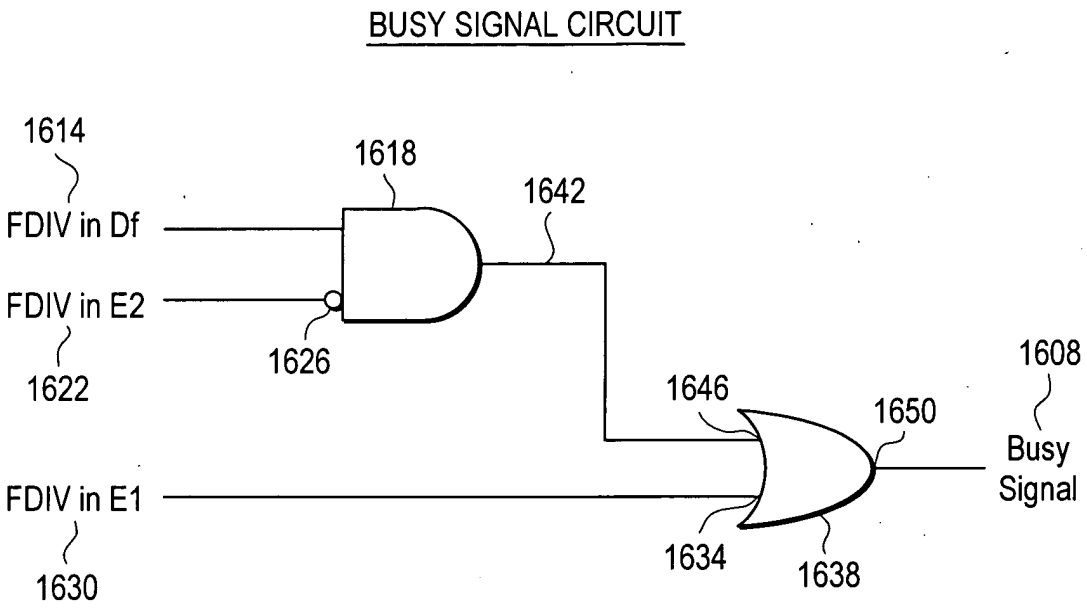

BUSY SIGNAL CIRCUIT
1614
FDIV in Df
FDIV in E2
1622
1618
1642
1626
1646
1650
1608
Busy
Signal
FDIV in E1
1630
1634
1638

FIG. 16

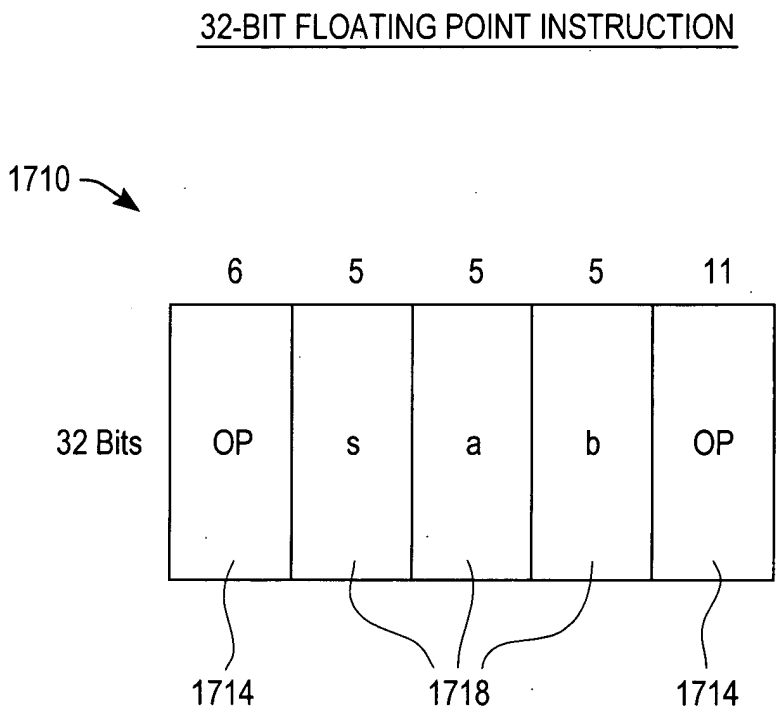


FIG. 17
(PRIOR ART)

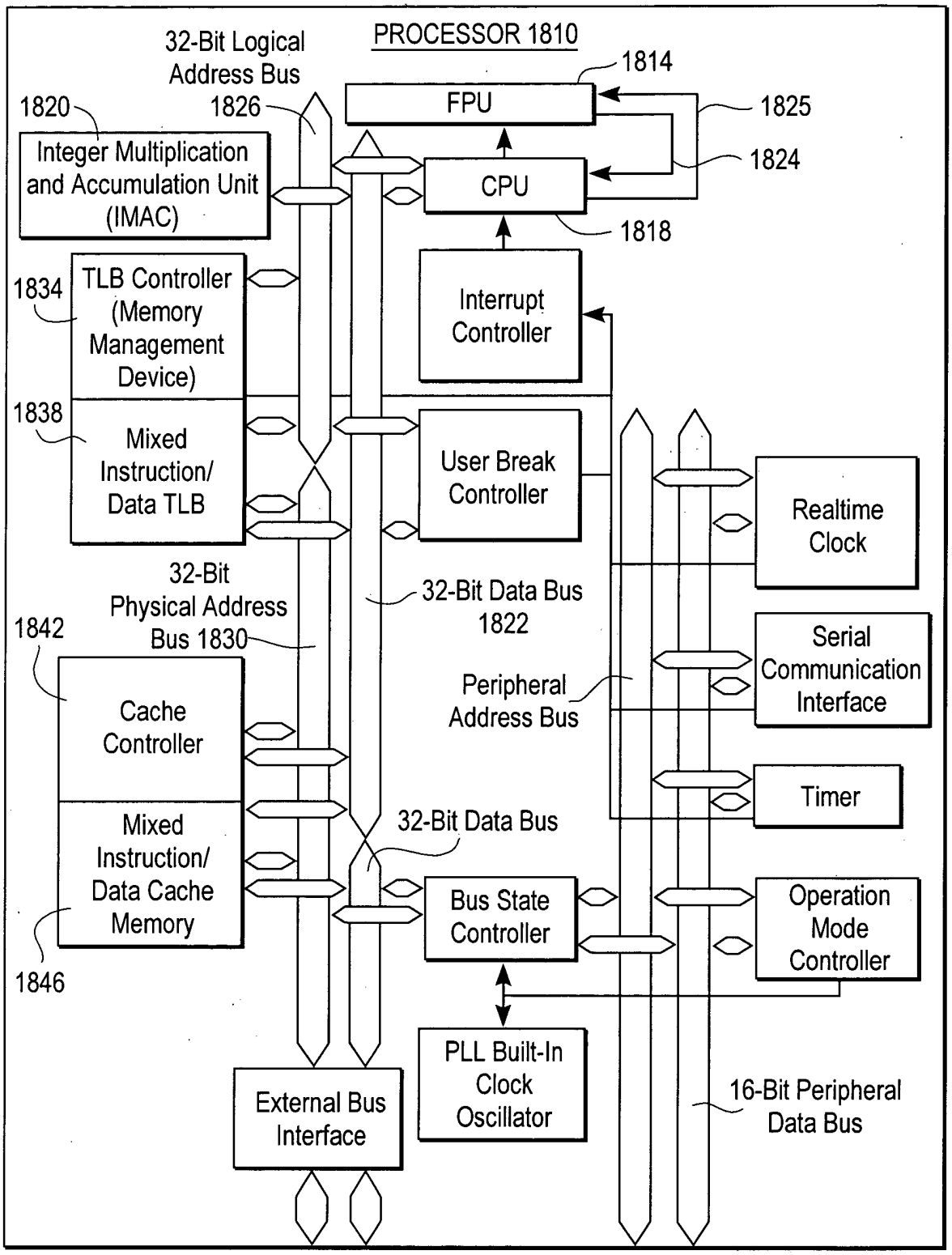

PROCESSOR 1810
32-Bit Logical Address Bus
1826
1814
FPU
1825
1820
Integer Multiplication and Accumulation Unit (IMAC)
1824
CPU
1818
1834
TLB Controller (Memory Management Device)
Interrupt Controller
1838
Mixed Instruction/ Data TLB
User Break Controller
Realtime Clock
32-Bit Physical Address Bus 1830
32-Bit Data Bus 1822
1842
Serial Communication Interface
Peripheral Address Bus
Cache Controller
Timer
32-Bit Data Bus
Mixed Instruction/ Data Cache Memory
Bus State Controller
Operation Mode Controller
1846
PLL Built-In Clock Oscillator
External Bus Interface
16-Bit Peripheral Data Bus

FIG. 18

FLUSHING DENORMALIZED NUMBER TO ZERO CIRCUIT

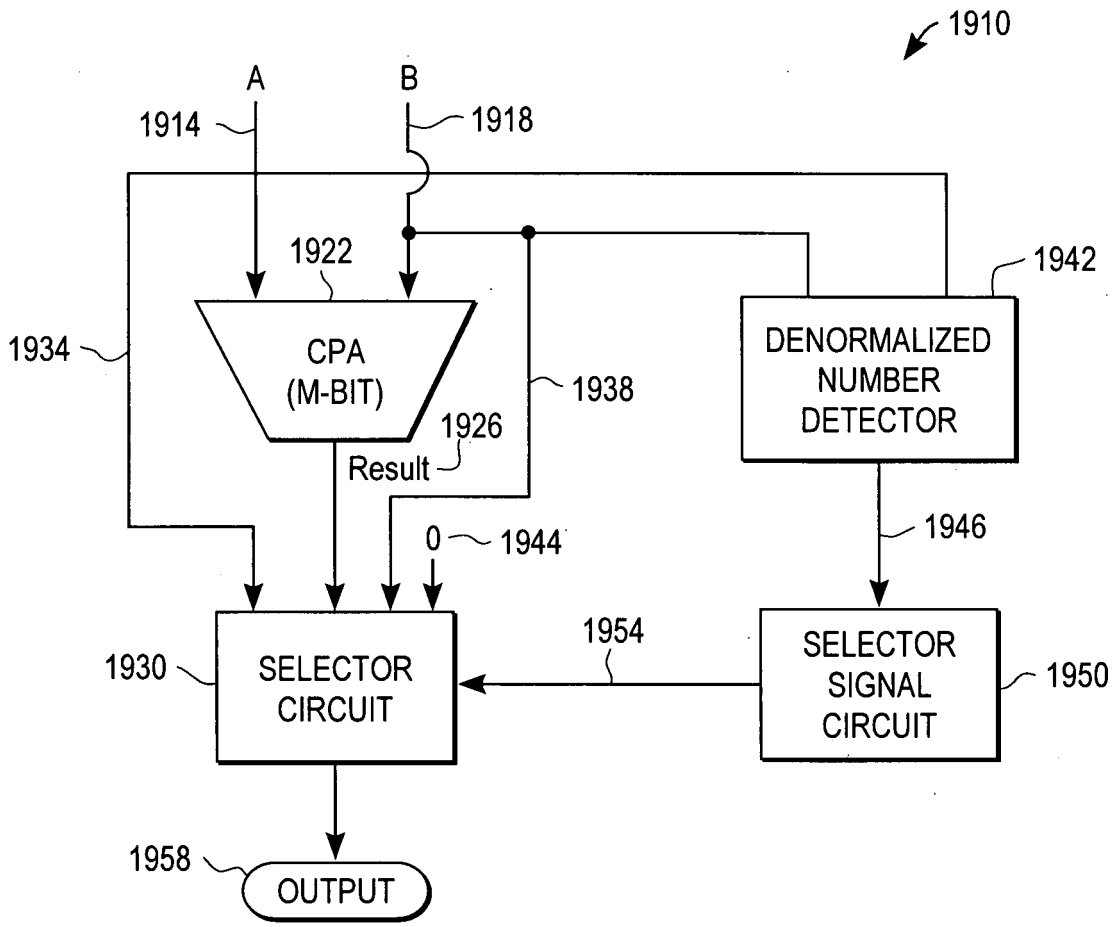


FIG. 19

DATA MOVEMENT TO AND FROM FPU

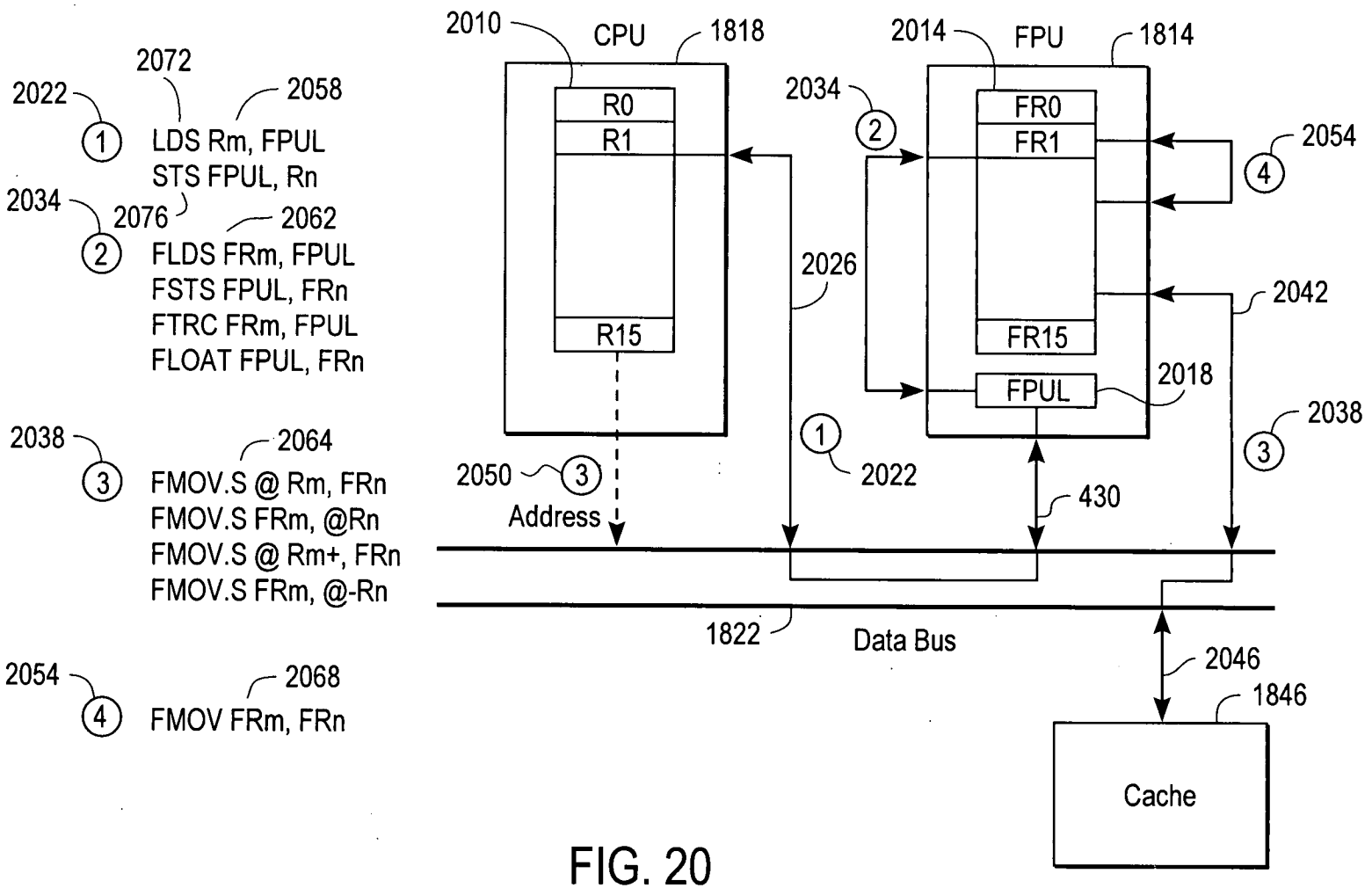


FIG. 20

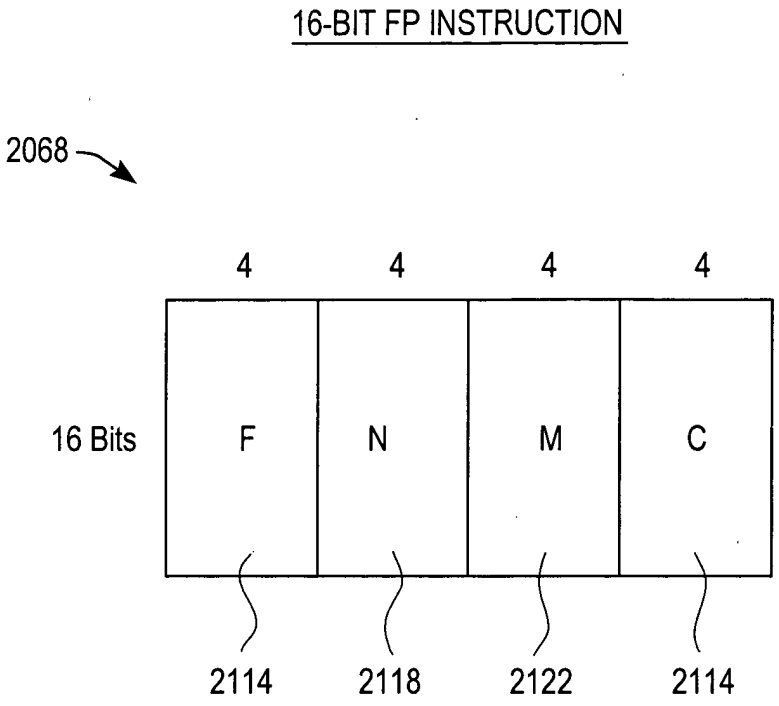

16-BIT FP INSTRUCTION
2068
4
4
4
4
16 Bits
F
N
M
C
2114
2118
2122
2114

FIG. 21

FPU AND CPU PIPELINES

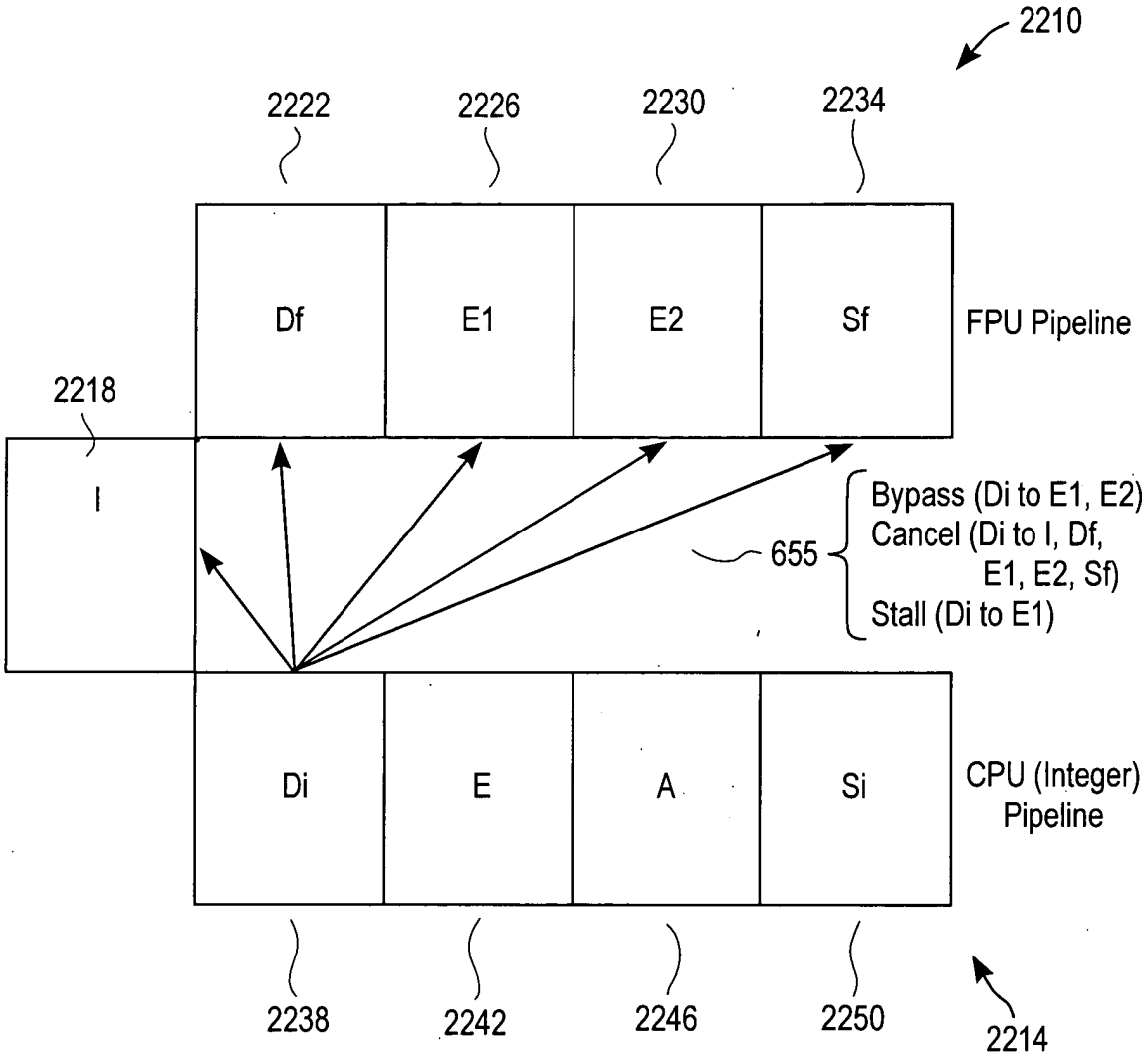


FIG. 22

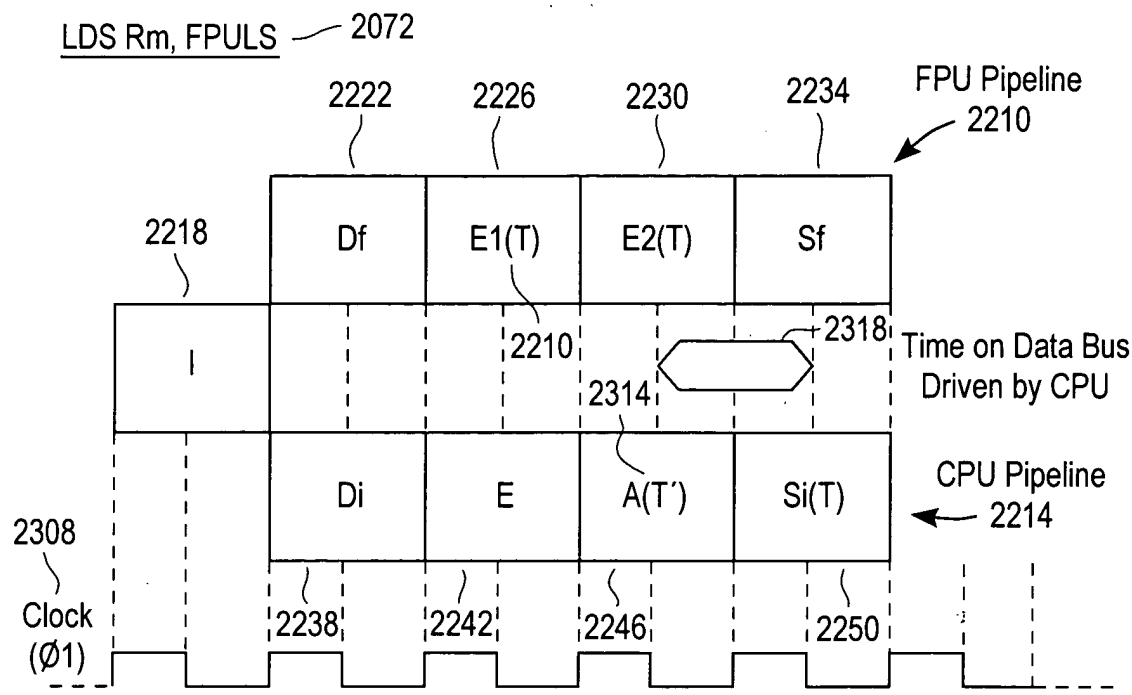


FIG. 23(a)

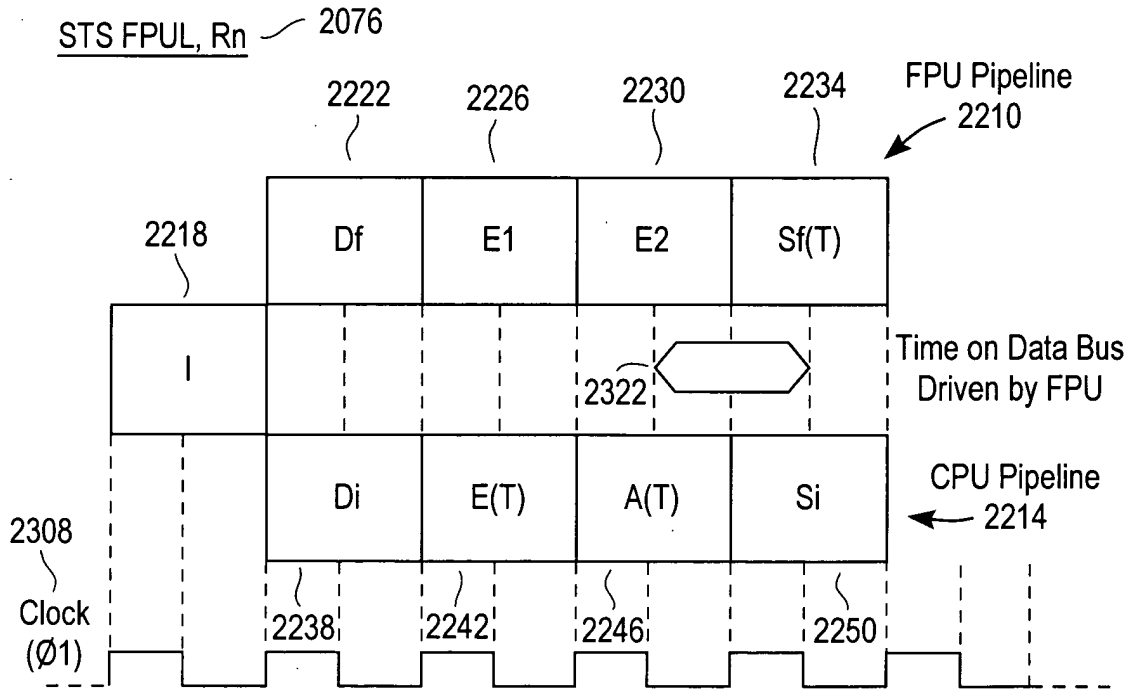


FIG. 23(b)

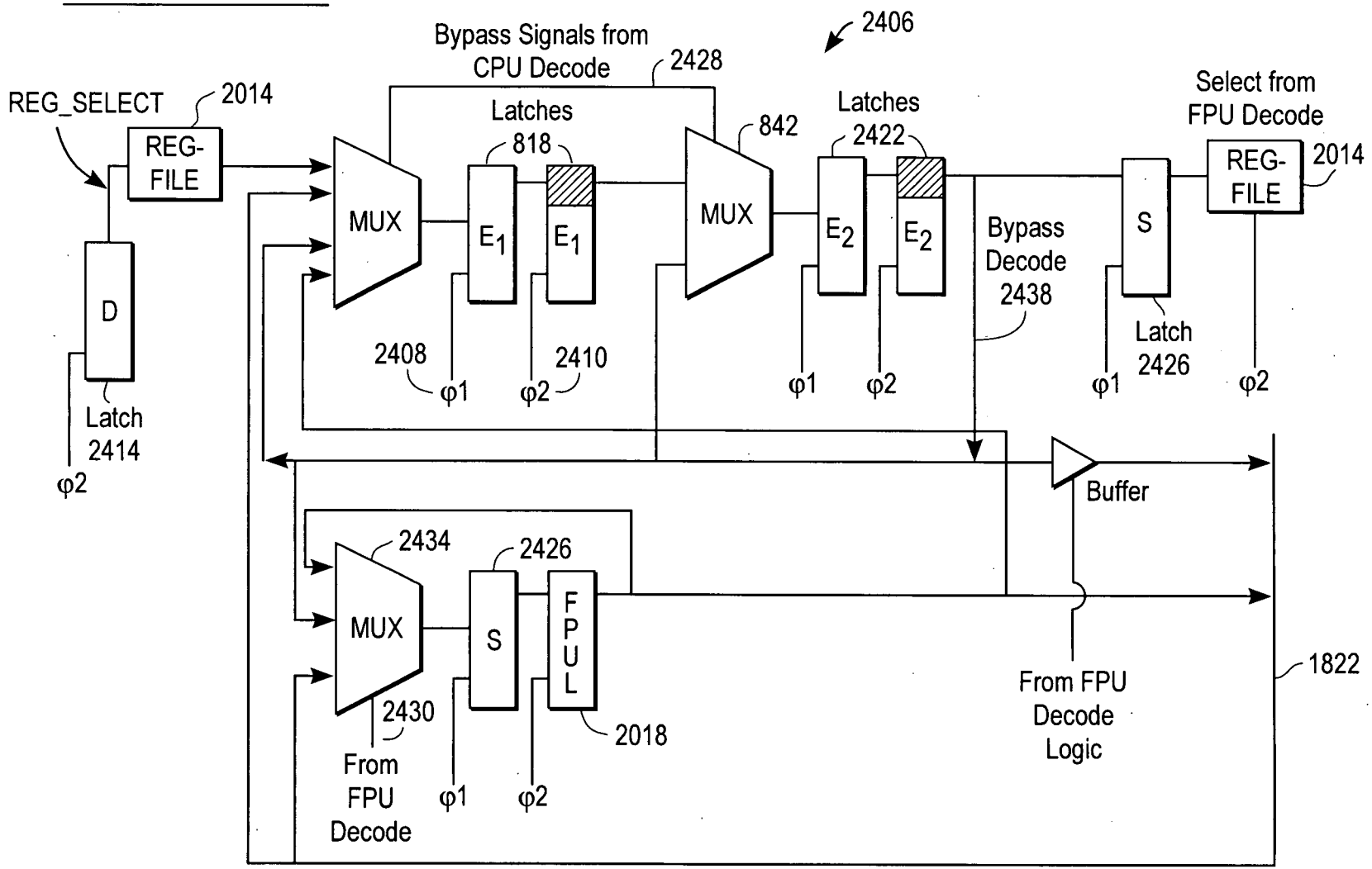

FPU PIPELINE CIRCUIT
2406
Bypass Signals from CPU Decode
2428
REG_SELECT
2014
REG-FILE
Latches
818
842
Latches
2422
Select from FPU Decode
REG-FILE
2014
MUX
E1
E1
MUX
E2
E2
S
D
Bypass Decode 2438
Latch 2426
Latch 2414
2408
φ1
2410
φ2
φ1
φ2
φ1
φ2
φ2
Buffer
2434
2426
MUX
S
FPUL
2430
2018
From FPU Decode
φ1
φ2
From FPU Decode Logic
1822

FIG. 24

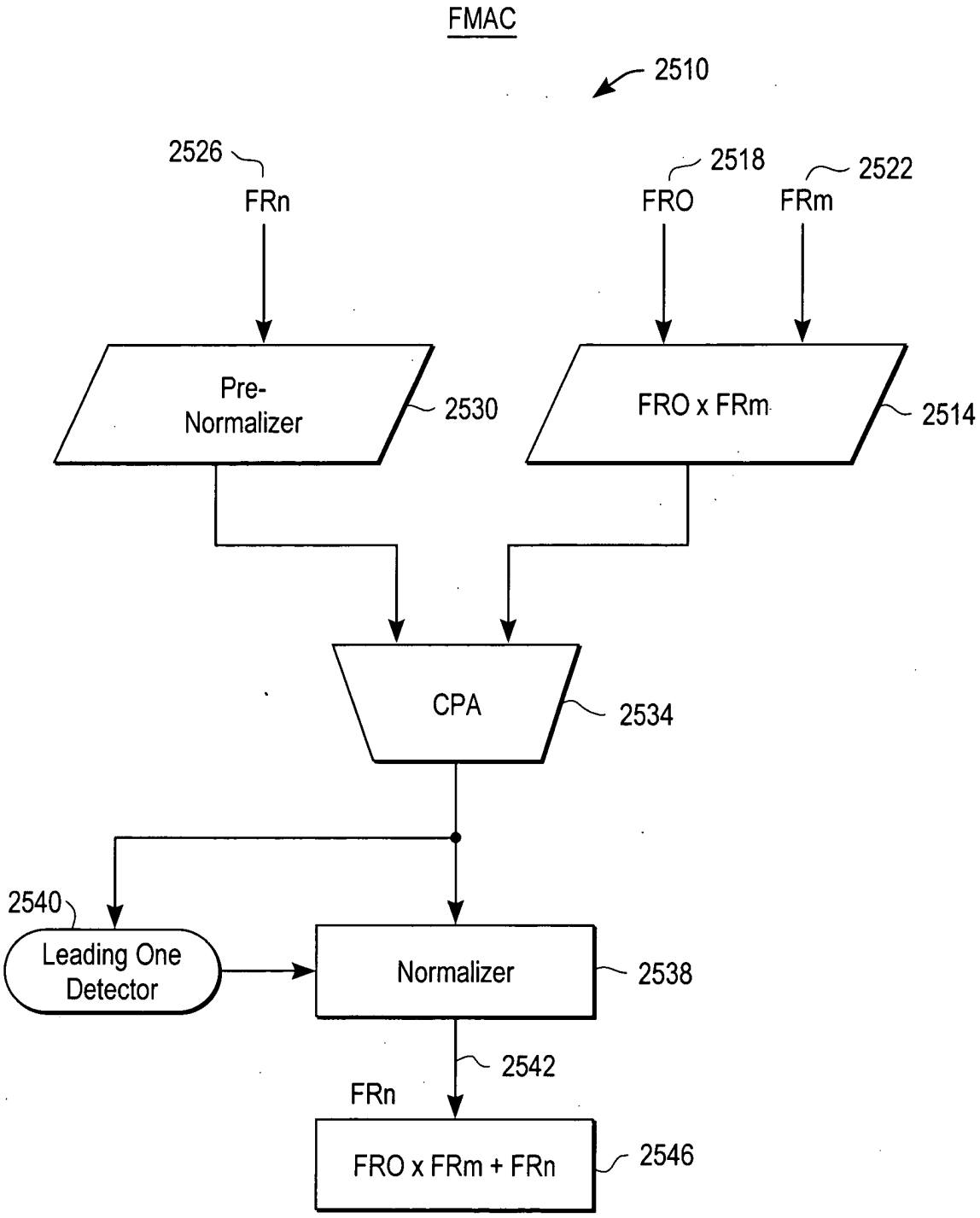

FMAC
2510
2526
FRn
2518
FRO
2522
FRm
Pre-
Normalizer
2530
FRO x FRm
2514
CPA
2534
2540
Leading One
Detector
Normalizer
2538
2542
FRn
FRO x FRm + FRn
2546

FIG. 25

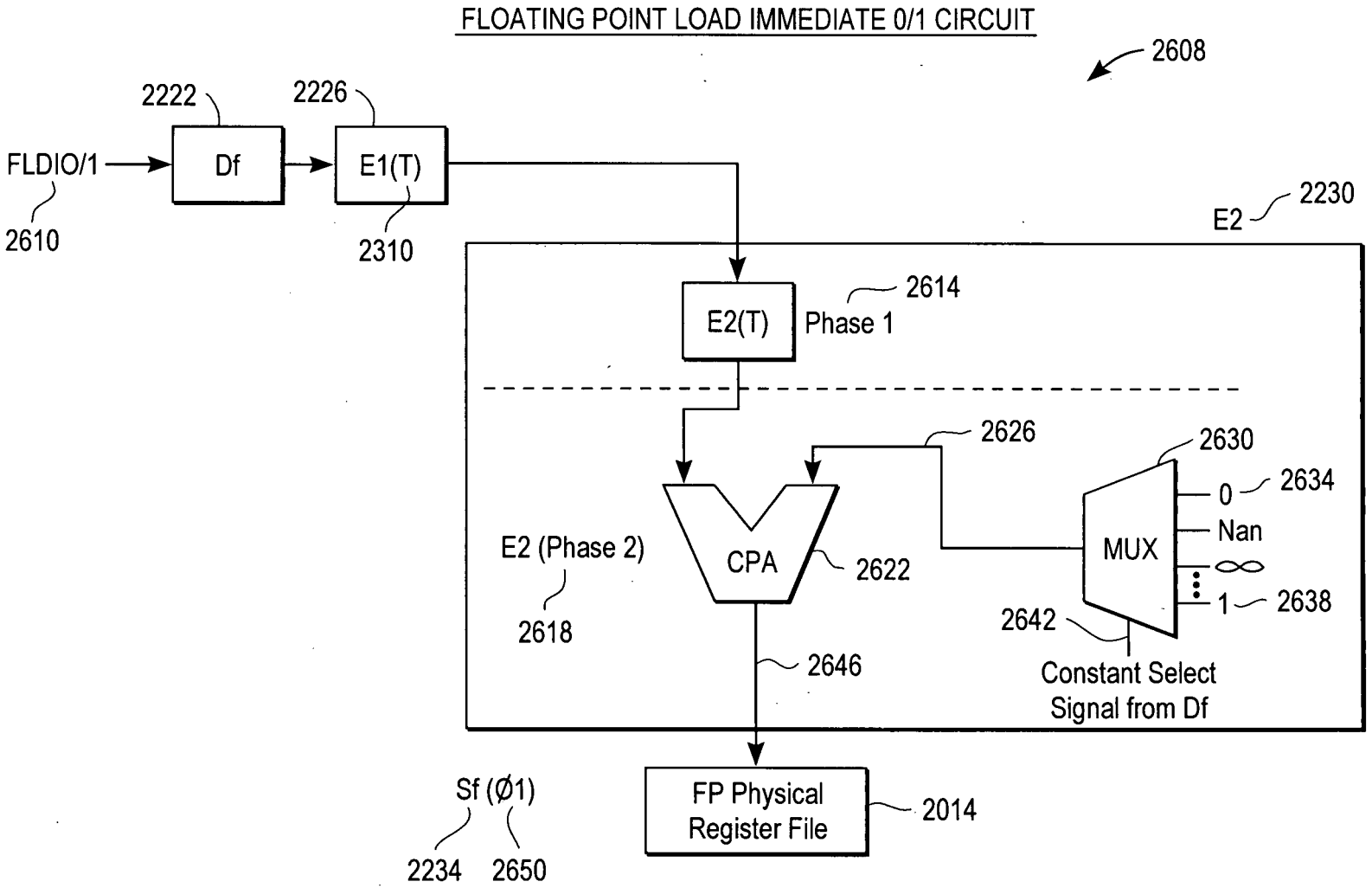

FLOATING POINT LOAD IMMEDIATE 0/1 CIRCUIT
2608
2222
2226
FLDIO/1
Df
E1(T)
2610
2310
E2
2230
E2(T)
Phase 1
2614
2626
2630
0
2634
Nan
MUX
E2 (Phase 2)
CPA
2622
1
2638
2618
2642
2646
Constant Select
Signal from Df
Sf (Ø1)
FP Physical
Register File
2014
2234
2650

FIG. 26

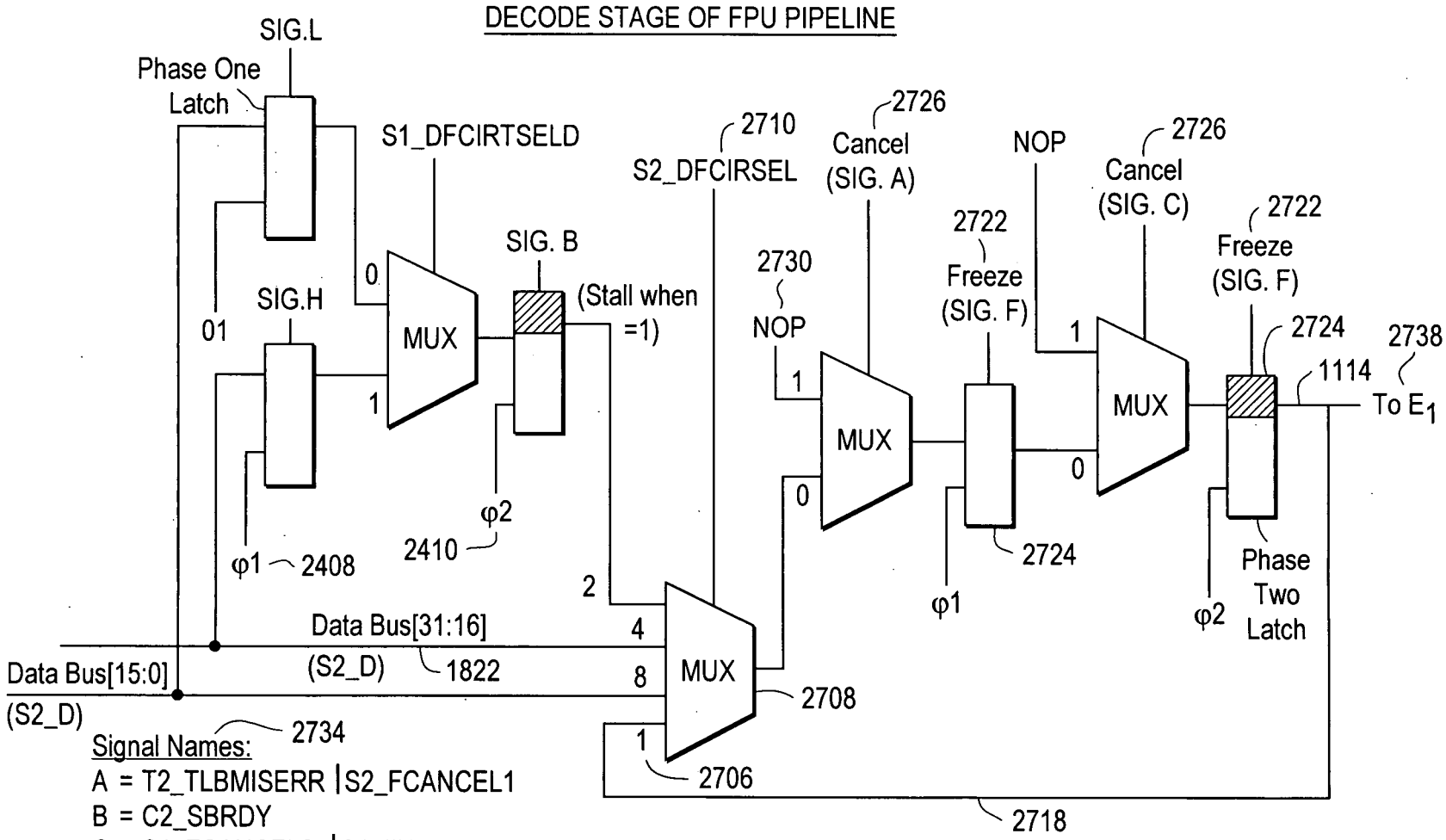
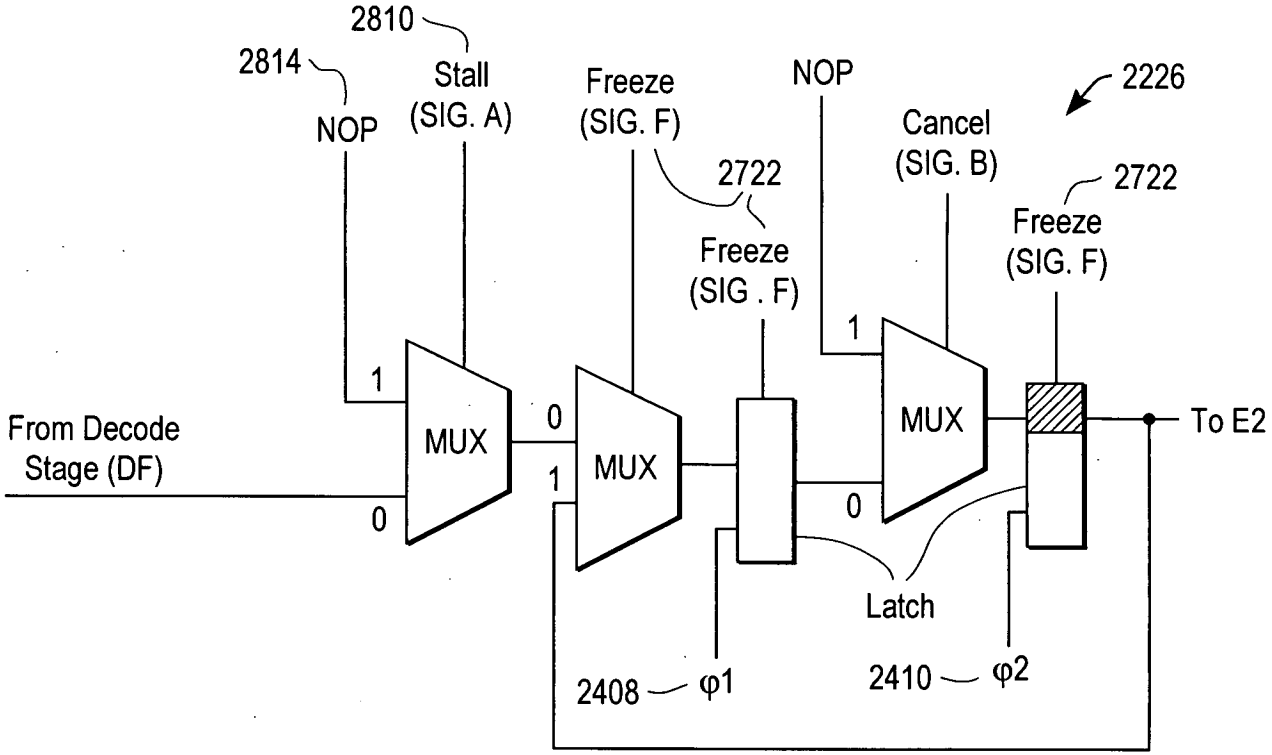

DECODE STAGE OF FPU PIPELINE
SIG.L
Phase One Latch
S1_DFCIRTSELD
2710
S2_DFCIRSEL
2726
Cancel (SIG. A)
NOP
2726
Cancel (SIG. C)
2722
Freeze (SIG. F)
SIG. B
(Stall when =1)
2730
NOP
2722
Freeze (SIG. F)
2724
1114
2738
To E1
SIG.H
01
MUX
MUX
MUX
MUX
φ1
2408
φ2
2410
φ1
2724
φ2
Phase Two Latch
Data Bus[31:16] (S2_D)
1822
Data Bus[15:0] (S2_D)
2734
2708
2706
2718
Signal Names:
A = T2_TLBMISERR |S2_FCANCEL1
B = C2_SBRDY
C = S1_FCANCEL2 |S1_IINVALID
F = (C2_SBRDY & L2_LRDY)
L = S2_IRTHILL & C2_SBRDY & L2_LRDY
H = S2_IRTHIHL & C2_SBRDY & L2_LRDY

FIG. 27

FIRST EXECUTIONS STAGE (E1) OF FPU PIPELINE



2814

Signal Names:

A = (T2_TLBMISERR & ~ FPU_IFETCH) |S2_FSTALL |~FDIV_STEP |(C2_SBRDY & L2_LRDY)

B = S1_FCANCEL2

F = (C2_SBRDY & L2_LRDY)

FIG. 28

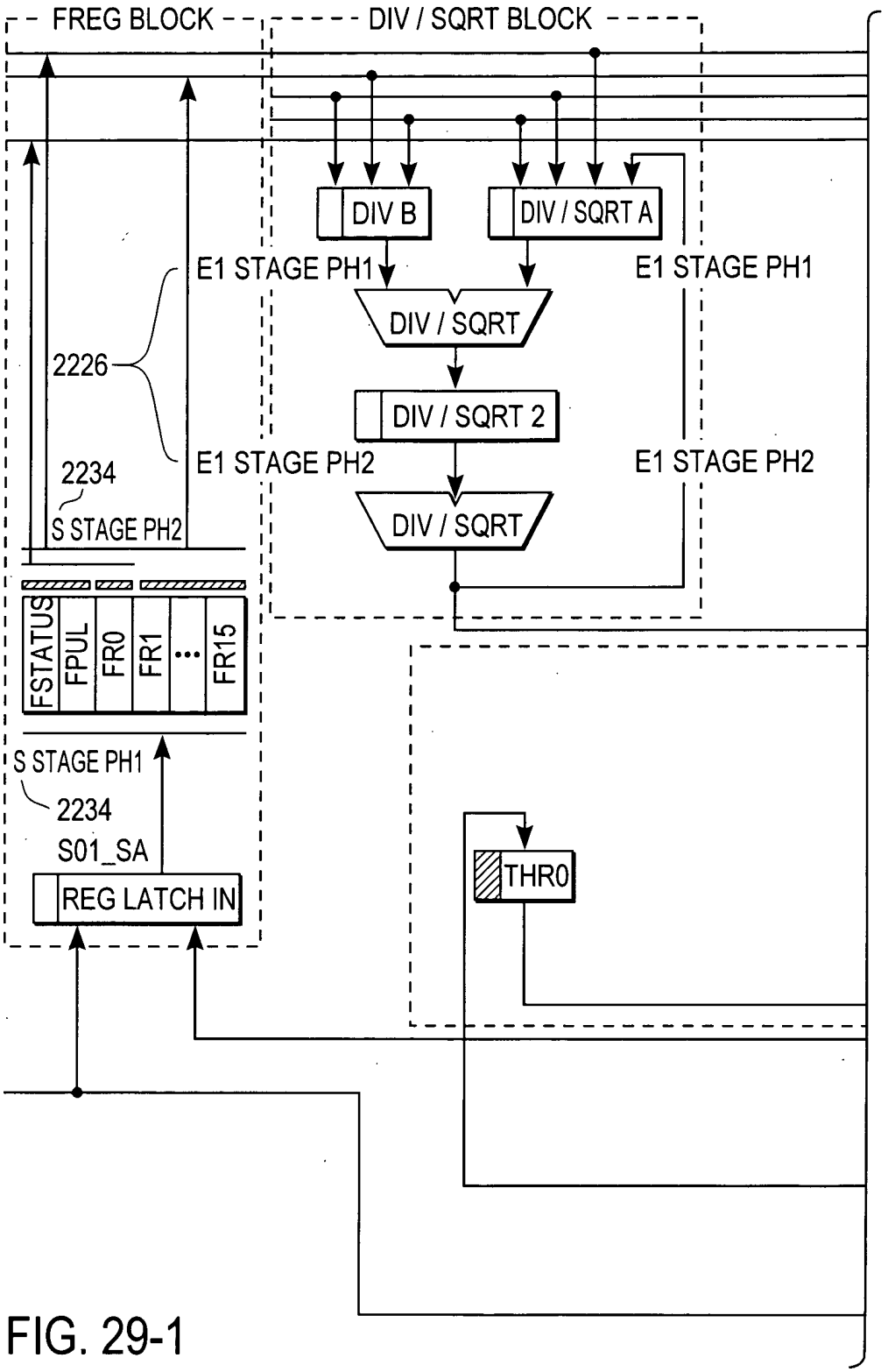
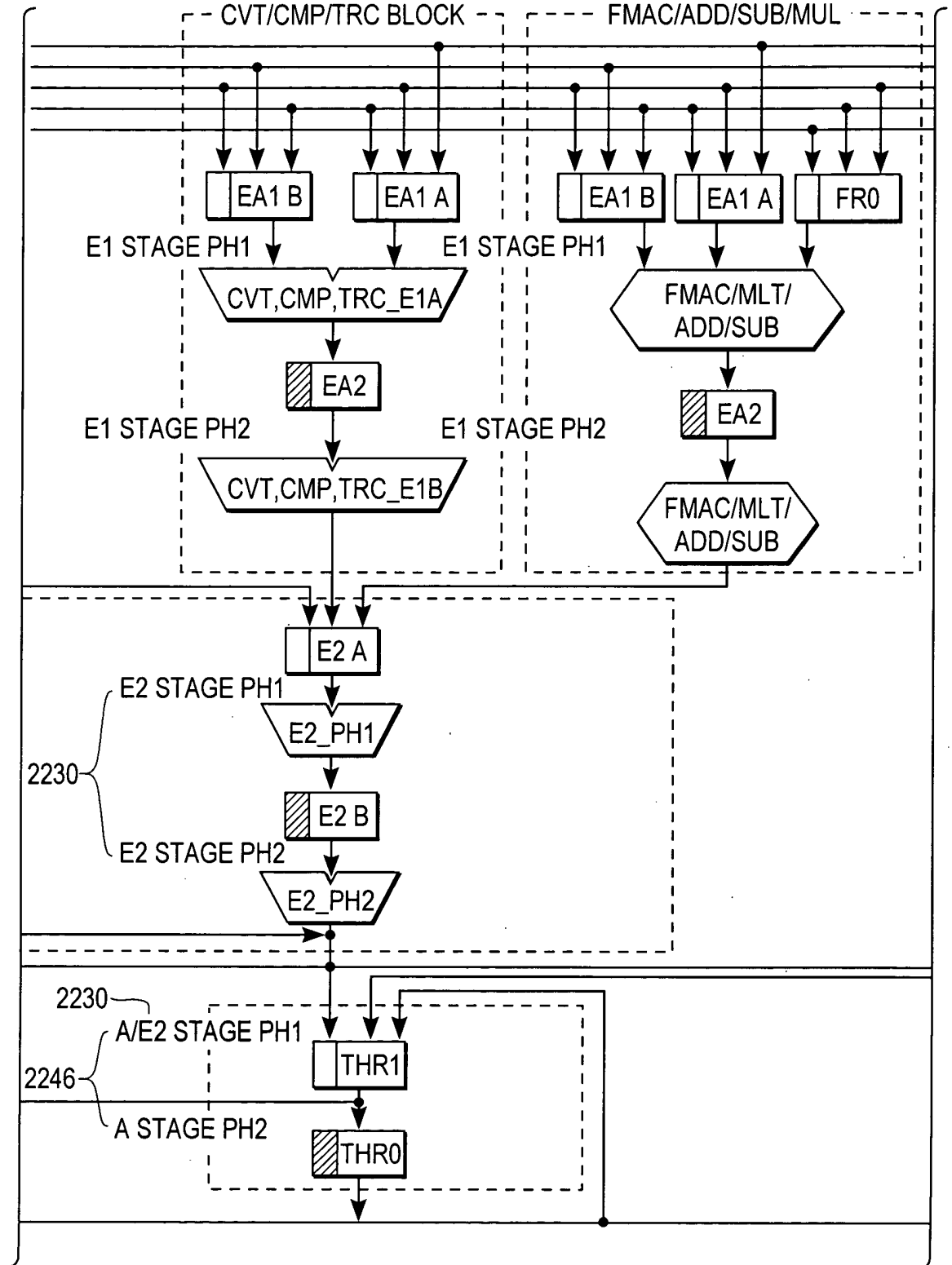


FIG. 29-1

FIG. 29-2 →



← FIG. 29-1

FIG. 29-2

FIG. 29-3 →

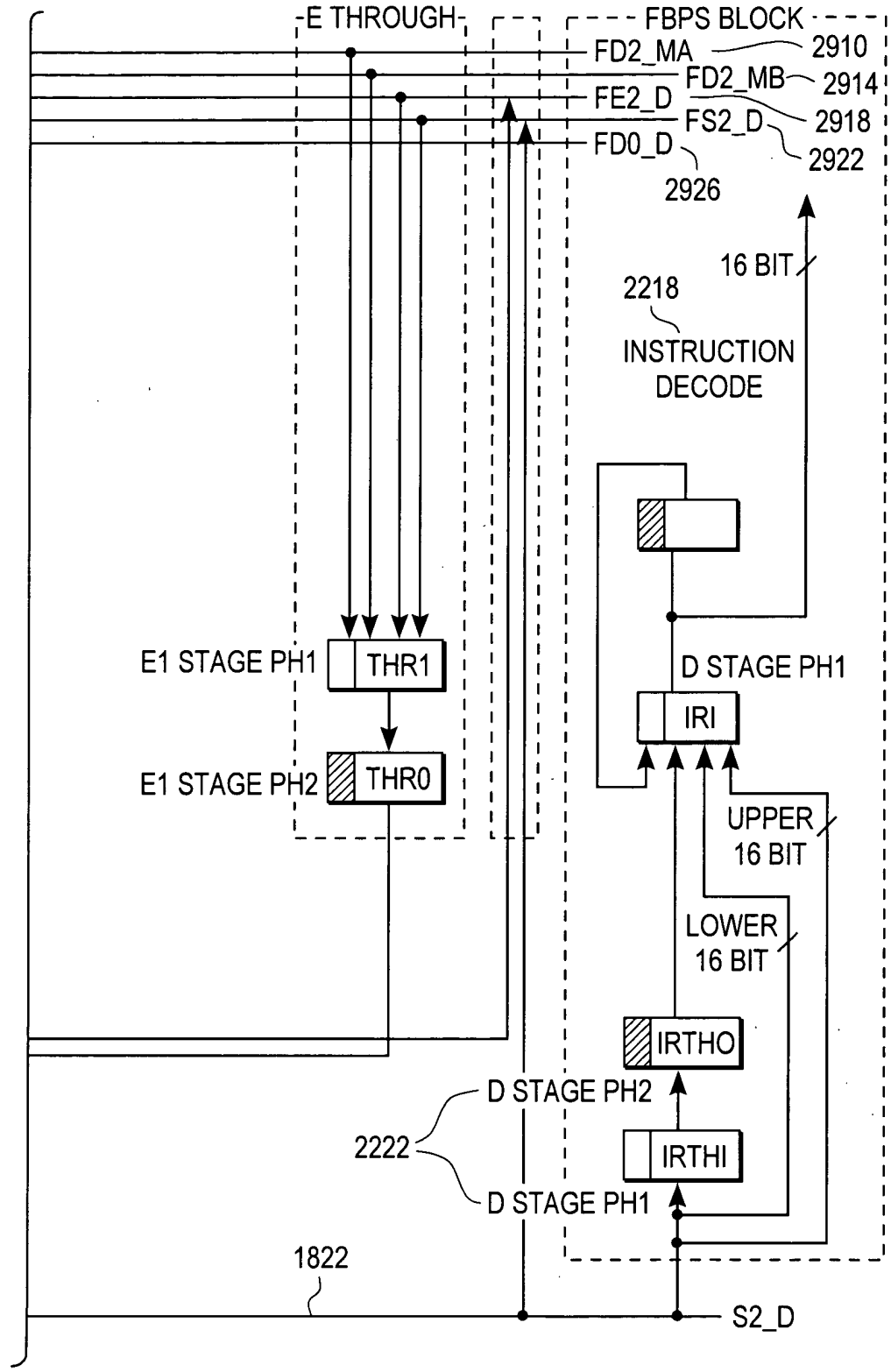

E THROUGH
FBPS BLOCK
FD2_MA
2910
FD2_MB
2914
FE2_D
2918
FS2_D
2922
FD0_D
2926
16 BIT
2218
INSTRUCTION DECODE
E1 STAGE PH1
THR1
E1 STAGE PH2
THR0
D STAGE PH1
IRI
UPPER 16 BIT
LOWER 16 BIT
IRTHO
D STAGE PH2
2222
IRTHI
D STAGE PH1
1822
S2_D
FIG. 29-2

FIG. 29-3

ROUNDING TO ZERO CIRCUIT

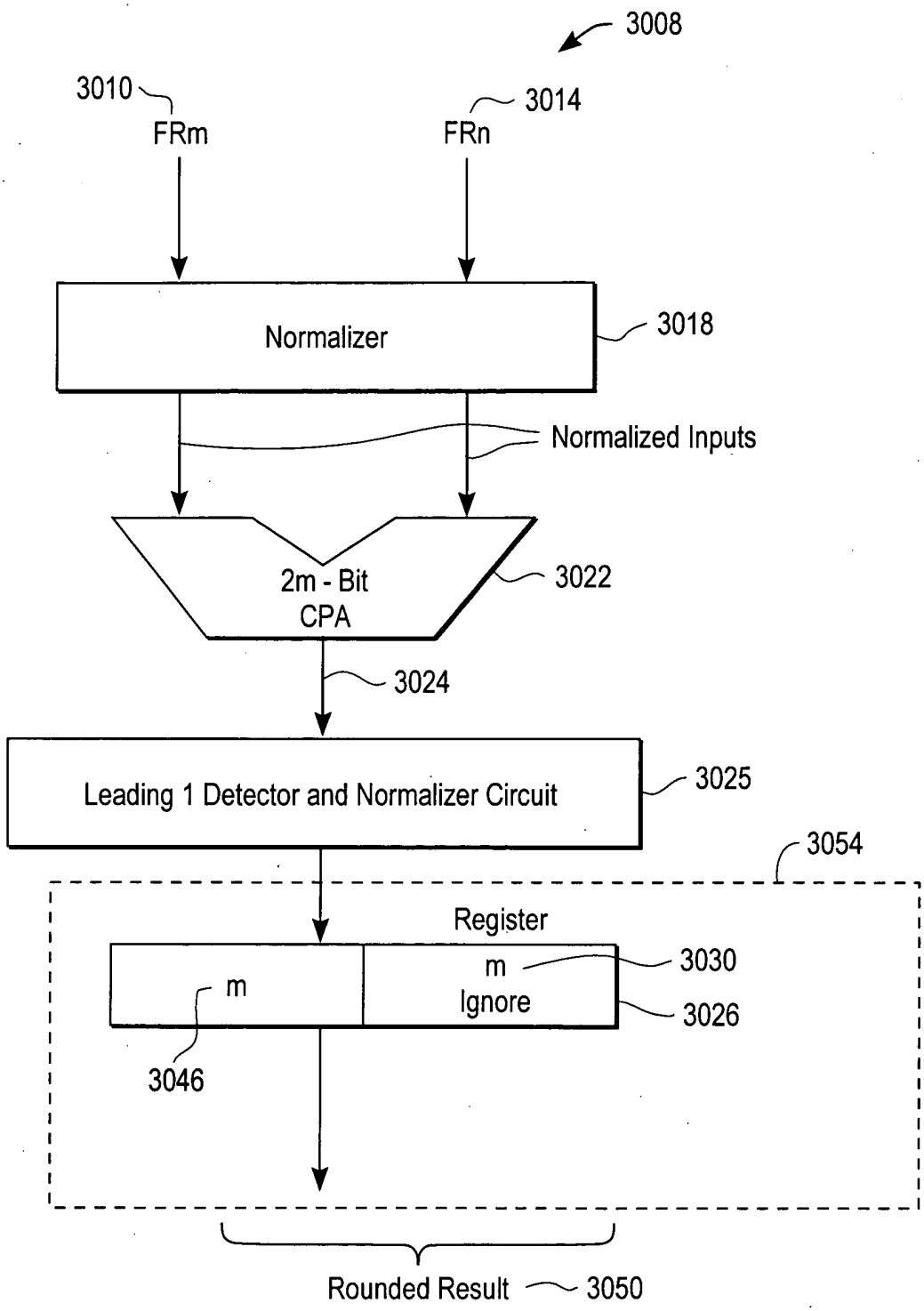


FIG. 30